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# Harmonic phase detector for phase locking of cryogenic terahertz oscillators

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We present a simple and effective way to phase lock terahertz cryogenic oscillators. Extreme nonlinearity of a superconductor-insulator-superconductor tunnel junction allows its implementation as a cryogenic high-harmonic phase detector (HPD), which is used both for mixing a terahertz oscillator signal with a microwave reference and for generating a phase error feedback signal that is directly applied to the oscillator for its phase locking. An integration of the HPD with a cryogenic flux-flow oscillator results in synchronization bandwidth as wide as 70 MHz (significantly exceeding conventional room-temperature system bandwidth), providing phase locking of 84% emitted power for 15 MHz oscillator linewidth. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4819064]

Frequency- and phase-stabilized terahertz oscillators have found a number of applications in different fields, including far-infrared astronomy and high-resolution molecular gas spectroscopy. Since sensitive terahertz (THz) mixers for these applications have to operate at cryogenic temperature to fulfill their performance potential, the development of compact cryogenic solid-state sources of THz radiation is important. An example of promising terahertz sources are quantum cascade lasers (QCLs),[1–6] operating at frequencies between 1.5 and 4.7 THz with emitted power levels up to tens of milliwatts. Phase locking of a terahertz QCL to a stable microwave reference has been proven for QCLs operating at 1.5 THz (Ref. 4) and 2.7 THz (Ref. 5).

Terahertz generation utilizing stacks of intrinsic Josephson junctions (IJJs) in the high-transition-temperature (high-$Tc$) cuprate $Bi_2Sr_2CaCu_2O_{8+\delta}$ (BSCCO) has also been much researched in recent years.[7–11] An IJJ is formed naturally in the BSCCO unit cell, with the $CuO_2$ layers forming the superconducting electrodes and the BiO and SrO layers forming the barrier layer.[12] A crystal of 1 $\mu$m thickness consists of ~670 IJJs. In 2007, it was discovered that such stacks can emit coherent radiation at frequencies up to 0.85 THz (Ref. 7). Recently, a total emission power as high as 30 $\mu$W was achieved, and the maximum emission frequency exceeded 1 THz at the fundamental mode.[11] Direct spectral measurements[13] have demonstrated wide tunability, good stability, and radiation linewidth well below 50 MHz for the BSCCO oscillator operating in a high bias regime.

Another cryogenic THz source, the Josephson Flux Flow Oscillator (FFO),[14] has proven[15] to be the most developed superconducting local oscillator for integration with a Superconductor-Insulator-Superconductor (SIS) mixer in a single-chip submillimeter-wave Superconducting Integrated Receiver (SIR).[16,17] The FFO is a long Josephson tunnel junction of overlap geometry in which an applied dc magnetic field (usually generated by a current in an integrated control line, $I_{CL}$) and a dc bias current, $I_B$, drive a unidirectional flow of fluxons, each containing one magnetic flux quantum. According to the Josephson relation, when the FFO is biased at voltage $V$, it oscillates with a frequency $f = (2e/h)V$ (about 483.6 GHz/mV), as a voltage control oscillator. The Nb-based FFO was the first Josephson oscillator phase-locked to the external reference;[18] this approach was used for the SIR implementation.[15–17] The FFO signal is down-converted by a cryogenic harmonic mixer integrated with the FFO in one chip. The amplified intermediate frequency (IF) signal is compared with a microwave reference signal by a conventional room-temperature phase-locking loop (RT PLL) system; a phase error signal is returned to control the FFO inside the cryostat.

Detailed measurements of the FFO linewidth[18] demonstrate a Lorentzian shape of the free-running FFO line (linewidth varies from 0.1 to some tens of MHz). This implies that the "natural" FFO linewidth is determined by combination of the wideband thermal fluctuations and the shot noise. The same Lorentzian shape of the free-running line was measured also for both QCL[3–6] and BSCCO[13] oscillators. However, while all the oscillators discussed above are based on various principles, they have some common features that require similar efforts for phase locking. The theoretical modeling of PLL systems has demonstrated that very wide-loop bandwidth (BW) is required for efficient locking of the Lorentzian line because of the slow decrease in power with an offset from the carrier.[19] To phase lock more than 90% of the power emitted by such an oscillator (required for most applications in radio astronomy and high-precision spectroscopy) the PLL BW should be seven times wider than a free-running linewidth (full width at half maximum), e.g., 70 MHz for linewidth of about 10 MHz.

As has been experimentally demonstrated, the PLL BW is inversely proportional to the time delay of the feedback loop.[20] The BW of the regular RT PLL, used for the FFO phase locking,[17] was limited to 14 MHz due to total delay of about 17 ns (7 ns contribution from the PLL filters and

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[a)] Electronic mail: kalashnikov@hitech.cplire.ru semiconductor electronics and 10 ns from 2 m-long cables connecting the RT PLL electronics with the cryogenic FFO). Traditional semiconductor PLL is not able to operate at 4 K level and should be placed outside of the cryostat. As a result, the minimal cabling length is restricted by cryostat size and cannot be significantly reduced without increasing the heat flux into the cryogenic space. Thus, the PLL BW expansion demands the development of a fully cryogenic PLL with a very fast phase detector that could be placed extremely close to the oscillator.

To overcome the limitations of the traditional RT PLL, the Cryogenic Phase Locking Loop (CryoPLL) system[20] was developed, which employs a cryogenic phase detector based on the SIS tunnel junction. All the elements of the CryoPLL are located very close to the FFO inside the cryostat to minimize the loop length, providing the BW of 40 MHz, which considerably exceeds the BW of the RT PLL. At the same time, for operation of the CryoPLL system an additional cryogenic amplifier is required, which makes implementation of the CryoPLL in the SIR array applications difficult. Furthermore, the achieved BW of 40 MHz is almost the limit value for this concept and cannot be considerably improved in the future.

In this paper we propose an approach for phase locking of cryogenic oscillators—a combination of the harmonic mixer and the phase detector in one SIS junction, which is a further extension of the CryoPLL concept. This element is called a cryogenic harmonic phase detector (HPD). In this approach, there are only superconducting elements in the phase-locking loop, allowing extreme compactness due to the absence of temperature gradients and negligibly small power dissipation. SIS junctions are obviously the best candidates for HPD implementation; previous experiments have proved their ability to operate as high harmonic mixers integrated with a cryogenic local oscillator,[18] as well as with a cryogenic phase detector with a negligibly small group delay.[20]

When the THz oscillator signal (frequency $f_{osc}$) and the stable microwave local oscillator (LO) signal $f_{LO} \approx f_{osc}/n$ ($n$—harmonic number) are applied to the HPD, the beat signal $I_{IF}(t) = I_{HPD}\sin(2\pi(f_{osc} - nf_{LO})t + \varphi)$ can be observed at the intermediate frequency, where the output current amplitude $I_{HPD}$ depends on the amplitude of the input signals and their frequencies. In the case of $f_{osc} = n\,f_{LO}$ the SIS junction works both as a harmonic mixer and as a sinusoidal phase detector. Its output signal can be applied directly to the oscillator in order to correct its phase and consequently to stabilize the frequency; this allows additional group delays to be avoided and provides a compact PLL system with the maximum possible BW. The error signal applied to the FFO control line is equal to

$$\varepsilon = G\sin(\varphi_{osc} - n\varphi_{LO}) = (2e/h)I_{HPD}R_d^{CL}\sin(\varphi_{osc} - n\varphi_{LO}), \tag{1}$$

where the $G$ is a loop gain expressed in the unities of frequency, $R_d{}^{CL} = \partial V_{FFO}/\partial I_{CL}$.

The PLL BW is defined by the Barkhausen stability criterion: $|W(s)| = 1$; $arg(W(s)) = \pi$, where $W(s)$ is a transfer function of a PLL loop, $s = j\omega$. For first-order PLL with the gain margin 3 dB this criterion is transformed to

$$BW\tau = 1/4, \tag{2}$$

$$G/BW = 1/\sqrt{2}, \tag{3}$$

where $\tau$ is a time delay. Formula (2) shows that the PLL BW is limited by the delay in the loop, and (3) defines the optimal gain for the given BW. For effective phase locking, the wide PLL BW—determined by loop delay—should, therefore, be realized in combination with sufficiently large PLL gain: $G = (2e/h)R_d{}^{CL}I_{HPD}$. We calculated the amplitude $I_{HPD}$ from the measured IF power of the HPD operating as a harmonic mixer with output signal frequency of about 6 GHz. It was found that both quasiparticle and Josephson nonlinearity can be employed for the HPD operation. The quasiparticle regime has already been thoroughly studied.[21,22] Nevertheless, we have used mainly the Josephson mode, since it provides 10–15 times larger output signal power despite a minor increase in noise level; this can probably be explained by the fact that oscillations in the SIS junction are completely synchronized by strong LO (see, for example, Ref. 23). Detailed studies of the HPD operation in the Josephson regime will be published elsewhere. Meanwhile, the results here show that the maximum output signal of the HPD based on the Nb–AlN–NbN SIS junction (area of 1.4 $\mu$m$^2$, gap voltage of 3.7 mV, current step at the gap of 180 $\mu$A) corresponds to $I_{HPD}$ of about 5 $\mu$A, which gives $G = 50$ MHz for typical $R_d{}^{CL} = 0.02\ \Omega$. According to Eq. (3) this gain is optimal for the PLL BW of about 70 MHz.

To prove the proposed HPD concept, we used the SIR microcircuit developed for the balloon-borne instrument TELIS (Terahertz LImb Sounder).[17] In this circuit, two SIS mixers are already integrated with the FFO; one of them can be used as the HPD while the second can be employed for the FFO spectrum monitoring. The simplified block diagram of the experiment is presented in Fig. 1. The output of the HPD is connected to the FFO control line via a low-pass filter and a 5 Ω resistor mounted on the FFO bias plate, providing a compact loop with group delay less than 4 ns. All the interconnections required for preliminary characterization of the elements, optimization of the HPD output signal and for the FFO phase locking by the regular RT PLL are shown in Fig. 1 by dashed-dotted lines. The HPD output signal power is optimized by tuning the LO power. Mostly even LO harmonic numbers were used, since they provide the maximum

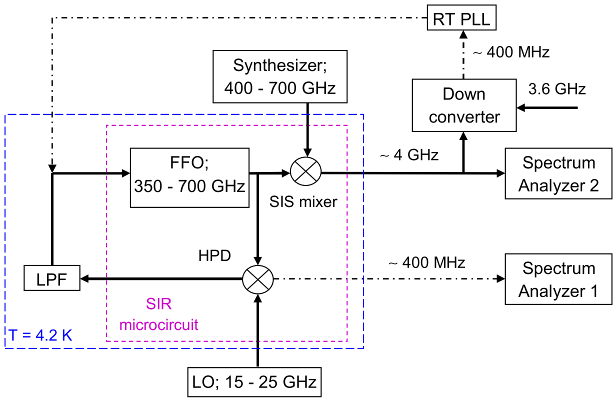

FIG. 1. Block diagram of the experimental setup for testing cryogenic harmonic phase detector.

output HPD signal at zero HPD bias, which is appropriate for practical application.

With this setup we can initially measure a linewidth of the FFO signal and even phase lock it by the RT PLL. A stable synthesizer signal and the FFO line are convoluted by the SIS mixer and down-converted to the intermediate frequency of about 4 GHz. The IF signal is applied to the RT PLL, which is also equipped with a frequency discriminator system with a relatively narrow bandwidth (<10 kHz) for frequency locking of the FFO. This narrow-band feedback system stabilizes the FFO mean frequency (although it does not affect the line shape), allowing accurate measurement of the free-running linewidth[18] (Fig. 2, dashed-dotted line). When a fast feedback branch of the RT PLL is switched on, the FFO become phase-locked (inset in Fig. 2, solid line). Note that all the reference sources used in the experiment were synchronized to a common 10 MHz reference.

In the crucial phase-locking experiment, the signals from the FFO and the LO are applied to the HPD and the frequency of the selected LO harmonic is chosen to be equal to the FFO frequency. In this case, the HPD generates a low-frequency output signal proportional to the phase difference between the FFO and the appropriate harmonic of the LO that is applied to the FFO control line for its phase locking. The spectrum of the FFO phase-locked by the HPD is depicted in Fig. 2 by a solid line. For a FFO line as wide as 15 MHz, the HPD is able to phase lock up to 84% of the emitted power; this is substantially more than the 4% synchronized by the regular RT PLL (see inset of Fig. 2). Synchronization bandwidth as high as 70 MHz can be worked out from the spectrum presented in Fig. 2.

The ratio of the phase-locked power to the total power emitted by the oscillator is called a "spectral ratio" (SR); this value characterizes a quality of phase locking. The SR is determined from a measured LO spectrum as a ratio of the phase-locked power of the carrier to the total emitted power including noise contribution from the mixer. So, the SR would be 100% for an ideal LO with a delta-shaped spectrum and zero phase noise level. Experimentally measured dependencies of the achieved SR on the free-running FFO linewidth are presented in Fig. 3 for three different PLL systems. It can be seen that the HPD concept provides not only simplicity and usability, but also offers superior performance, resulting in a SR value considerably higher than that which can be achieved with other approaches.

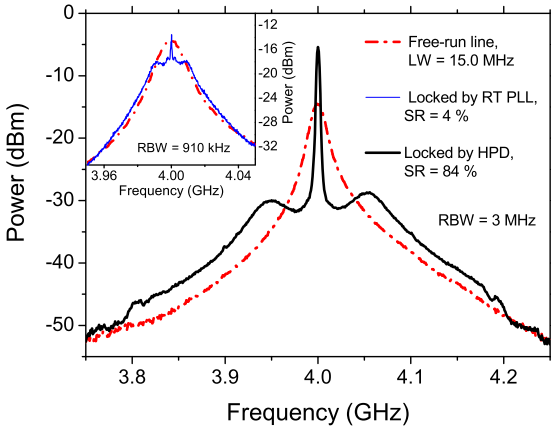

FIG. 2. Down-converted spectra of the FFO operating at 644 GHz in different regimes: Frequency locked (dashed-dotted line) and phase-locked by the HPD (solid line). The spectra of the same FFO line obtained in phase locking by the RT PLL are shown in the inset for comparison. Resolution bandwidths (RBWs) of the spectrum analyzer = 3 MHz.

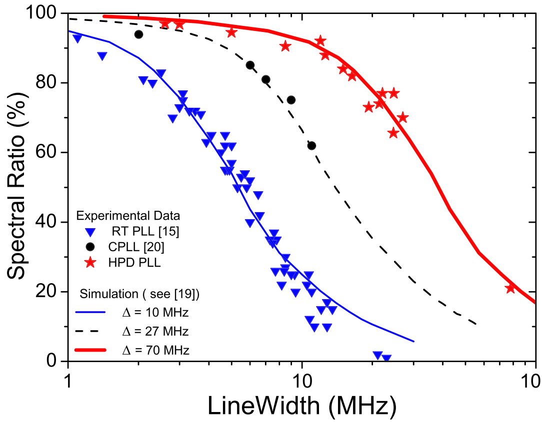

FIG. 3. Dependence of the spectral ratio on the free-running FFO linewidth measured for three different types of the PLL system. The SRs obtained in this work (asterisks) are compared with data for RT PLL (see Refs. 15, 18, and 19) and CryoPLL (Ref. 20). Results of calculation (Ref. 19) are shown by lines for different values of second-order PLL bandwidth Δ.

To demonstrate the ultimate performance of the HPD we used very wide FFO lines that were realized at the transition between low and high damping regimes, which occurs at the "boundary" voltage $V_b = V_g/3$ ($V_g$ is the gap voltage of the FFO) due to the effect of Josephson self-coupling.[24] This effect is caused by absorption of ac Josephson radiation by the quasiparticles and consequent photon-assisted tunneling. This results in current bumps at $V_{JSC} = V_g/(2n+1)$ with high differential resistance $R_d$ (and consequently wide FFO linewidth); on the other hand, in this region the $R_d^{CL}$ is also very high, leading to the large loop gain.

The utilization of an additional SIS mixer for synchronization monitoring makes the receiver too complicated and inconvenient for practical applications. In order to overcome this problem we developed a simple and effective method to observe a synchronization event and optimize the amplitude of the feedback signal. When the difference between $f_{osc}$ and $nf_{LO}$ is within the PLL bandwidth, the feedback system compensates the frequency difference and the HPD DC bias is changing that provides an indication of phase-locking. The HPD bias variation on the frequency offset $f_{osc} - nf_{LO}$ for different LO power levels is presented in Fig. 4. Thus, the synchronization event will be registered and the exact FFO frequency can be determined by monitoring of the HPD bias during the LO frequency sweep. This measurement can also be used for optimization of the loop gain by LO power changing, because the dependence of the dc response amplitude on the LO power coincides well with variation of the HPD output signal, independently measured in a harmonic mixer regime (see inset in Fig. 4).

The further increasing of the loop gain is required for optimal phase locking of narrow FFO lines below 5 MHz and for decreasing phase noise near the carrier. This can be done by enlarging the HPD output signal (increasing of the SIS junction area and its current density) and/or by using

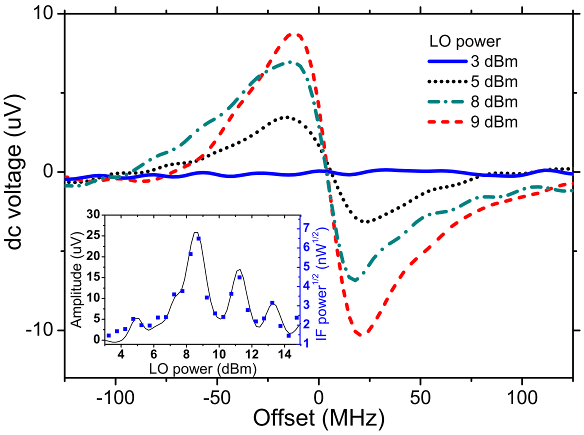

FIG. 4. Low-frequency response of the HPD output signal for different LO power values, measured with a low pass (15 Hz) filter; the HPD is biased around zero. The dependencies of the dc response amplitude (solid line, left axis) and the square root of the HPD output power (bars, right axis) versus LO power are shown in the inset.

superconducting dc amplifiers with extremely small power consumption.[25–28]

To summarize, in this work we have proposed and tested a superconducting element—the Harmonic Phase Detector based on an SIS tunnel junction. The HPD concept has been experimentally verified by phase locking of the FFO; a PLL BW as wide as 70 MHz has been experimentally realized that allows phase locking of up to 92% of power emitted by the FFO for 12 MHz free-running linewidth; almost 70% was synchronized for a 30 MHz line. The achieved results are important for the development of SIR arrays with FFOs phase-locked by the HPDs, as well as application of the SIR for very long baseline radio interferometry, where extremely high SR and low phase noise are required. The HPD concept could also be implemented for BSCCO oscillator phase locking, where development of extremely wide synchronization BW (>50 MHz) is vital; this could only be achieved by using the HPD.

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