Cryogenic Phase Locking Loop System for Flux-Flow Oscillator

A.V. Khudchenko, V.P. Koshelets, P.N. Dmitriev, A.B. Ermakov, O.M. Pylypenko

***Abstract*—We present an ultra wideband Cryogenic Phase Locking Loop system (CPLL). The CPLL has been developed for phase locking of a Flux-Flow Oscillator (FFO) in a Superconducting Integrated Receiver (SIR). The main element of the CPLL is a cryogenic phase detector (CPD) based on a superconductor – insulator – superconductor (SIS) tunnel junction. All the loop elements are placed at 4.2 K inside a cryostat with the FFO; so the novel CPLL system has a loop length only 50 cm. The CPLL operating frequency has been increased from 400 MHz up to 4 GHz to decrease a loop filter delay to 0.5 ns. As a result the total loop group delay is about 4.5 ns. Such a small delay results in a CPLL synchronization bandwidth as wide as 40 MHz and allows to phase-lock more than 60% of the emitted by FFO power even for FFO linewidth about 11 MHz. This fraction of phase-locked power is three times large than can be achieved with conventional room-temperature PLL. We have realized an integrating loop filter for the CPLL. Such a filter sufficiently increase stability and decrease a phase noise of the FFO phase-locked by the CPLL.**

I. INTRODUCTION

A Superconducting Integrated Receiver (SIR) [1], [2] comprises in one microcircuit a low-noise SIS mixer with quasioptical antenna, a Flux Flow Oscillator (FFO) acting as a Local Oscillator (LO) and a second SIS harmonic mixer (HM) for the FFO phase locking. The concept of the SIR looks very attractive for many practical applications due to SIR compactness and a wide tuning range of the FFO. For example, the SIR developed by SRON and IREE for TELIS [2] has been able to measure the ozone depleting component brome oxide in the stratosphere from a gondola of high–altitude balloon. The balloon was launched from Esrange (Sweden) in March 2009; it made a successful flight of 12 hours on 30 kilometers altitude. The SIR channel provided valuable scientific data during the whole flight; these data are under elaboration right now.

II. FLUX FLOW OSCILLATOR PHASE LOCKING

The FFO radiation spectrum was found to be the Lorentz line [3] at the frequencies up to 750 GHz. The free-running ("natural") FFO linewidth may be up to 10 MHz. Thus, for higher spectral resolution, a specially designed wideband semiconductor room temperature PLL (RT PLL) with synchronization bandwidth (BW) of about 12 MHz is used. The wider PLL BW is, the more power of the FFO can be phase-locked. The ratio between the phase-locked and the total power emitted by the oscillator is a so-called "spectral ratio" (SR). The RT PLL provides SR value around 50% for the 5 MHz wide FFO radiation line.

There are two main reasons to extend the BW of the PLL system to values much higher than the present 12 MHz. The first reason is that linewidth of the FFO's based on NbN or NbTiN films (that are the most attractive for future SIR applications at the frequencies of around 1 THz) can considerably exceeds 10 MHz due to higher surface losses. In this situation the PLL's bandwidth has to be as large as 50 MHz (to reach at least 50% of the SR value desirable for most applications). The second reason is that using an SIR for interferometry applications requires an LO with extremely high phase stability. For example, for the ALMA project the LO rms phase noise should be considerably less than 75 fs (the value of rms atmospheric fluctuation in location of the interferometer) [4]. The SR > 95 % is required for this rms phase noise level at the frequency of about 600 GHz. To provide such a large SR value even for the FFO with relatively small linewidth of 2 MHz, the PLL should have BW of about 50 MHz.

III. CONCEPT OF THE CRYOGENIC PLL SYSTEM

The BW is determined by the group delay τ in the loop; for RT PLL the BW is limited to 12 MHz because the total delay is about 15 ns (including 5 ns contribution from the PLL filters and semiconductor electronics and 10 ns from the 2 m long cables connecting the RT PLL with cryogenic FFO). The minimal cabling length is restricted by the size of a cryostat and cannot be essentially reduced without increasing the heat flux into the cryogenic space. Note that the traditional PLL is a semiconductor-based device designed for 300 K, and it cannot be placed directly in the cryostat.

So, to overcome the limitation of the RT PLL we propose a concept of the CPLL based on a Cryogenic Phase Detector (CPD) [5]-[7]. All elements of the CPLL are placed very close to the FFO inside the cryostat to avoid any temperature gradients between FFO and phase detector and to minimize the loop length. Negligible CPD delay and small time delays in the short loop lead to ultra wide BW. The proposed concept has been realized and the CPLL has been successfully tested [5] - [7]. The CPD properties and coupling between the CPD and the FFO were studied in detail [6], [7].

Manuscript received 6 May 2009. This work was supported in part by the RFBR projects 09-02-00246 and 09-02-12172 ofi-m, the ISTC project # 3174, and the Grant for the Leading Scientific School 5408.2008.2.

A. V. Khudchenko, V. P. Koshelets, P. N. Dmitriev and A. B. Ermakov are with the Kotel'nikov Institute of Radio Engineering and Electronics, Russian Academy of Science, 11/7 Mokhovaya St., 125009, Moscow (e-mail: Khudchenko@hitech.cplire.ru)

A. V. Khudchenko, V. P. Koshelets and A. B. Ermakov are also with SRON Netherlands Institute for Space Research, P.O. Box 800, 9700 AV Groningen, the Netherlands.

O. M. Pypypenko is with the State Research Center of Superconducting Electronics "Iceberg", Kyiv, Ukraine.

IV. Experimental Results

The previous realization of the CPLL is presented in [7]. This system has the length of the loop 1 m. The delay in filter is about 1.5 ns. There is also a delay 1 - 1.5 ns in other elements of the loop. So the total delay τ is 7 - 8 ns (compare to 15 ns for the RT PLL). This reduction of the τ results in increasing of the BW from 12 MHz to 25 MHz (see Fig. 1 curve 3). At the FFO linewidth of 10.8 MHz this CPLL is able to phase-lock 50% of the FFO power, compare to 23% for the RT PLL.

These successful results encourage us for further attempts to reduce total delay in the loop. Firs of all we decrease further the loop length down to 50 cm that corresponds to delay 2.5 ns. As the next step we considerably increase operational frequency of the system: from 400 MHz to 4 GHz. This modification leads to minimization of a band-stop loop filter group delay due to smaller values of reactive elements needed to realize required filter reflection. The delay in this new filter is about 0.5 ns.

Reduction of the loop delay due to latest changes results in increasing of the CPLL BW up to 40 MHz (Fig. 1 curve 2). For the FFO linewidth of 2 MHz this CPLL is able to phase-lock 94% against 82% for the RT PLL. Even more considerable gain was obtained at larger free-running FFO linewidth (see Fig. 1): SR = 63 % by the CPLL against 23 % for the RT PLL.

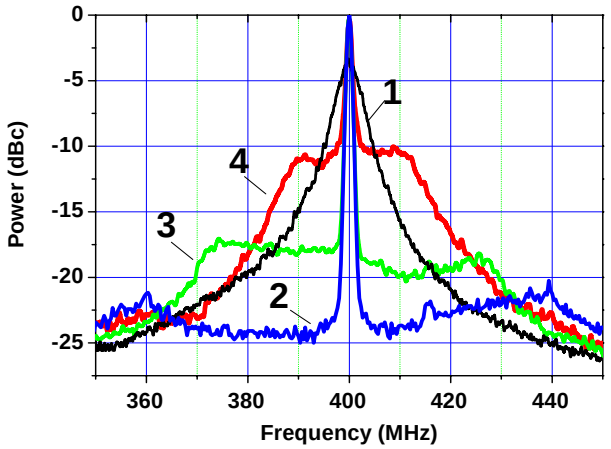

Fig. 1. Down-converted spectra of the FFO operating at 600 GHz: curve "1" – autonomous, linewidth 10.8 MHz; "2" – phase-locked with CPLL, BW 40 MHz (SR = 63%); "3" - phase locked with CPLL, BW 25 MHz (SR = 50%); "4" – phase-locked with RT PLL, BW 12 MHz (SR = 23%).

From the Fig.1 one can see that increasing of the PLL BW leads to extension of the frequency range, where phase noise of the PL FFO is lower than level for the free-running FFO. The wider BW of the CPLL enables us to use a larger gain that results in considerable decrease of phase noise in entire regulation bandwidth.

We have realized an integrating loop filter for the CPLL by placing it between the CPD and the FFO. Such a filter sufficiently increases stability. The integrating loop filter also considerable decreases a phase noise of the phase-locked FFO near the carrier at frequencies offset less then 100 kHz (see Fig. 2). The essential moment is that the filter is based on a passive elements operating at 4.2 K and can be placed close to the FFO and the CPD that keeps within the CPLL concept.

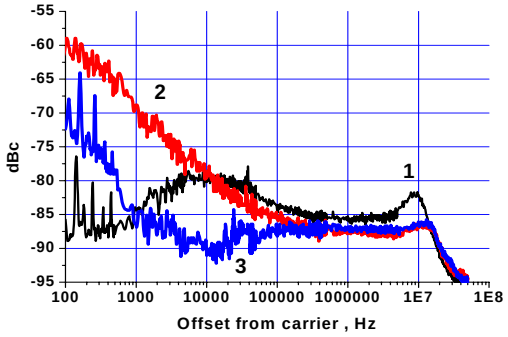

Fig. 1. Phase noise of the FFO phase-locked with: "1" –RT PLL; "2" – CPLL without integrating loop filter, BW 40 MHz (SR = 63%); "3" - CPLL with integrating loop filter.

V. Conclusion

Ultra wideband Cryogenic Phase Locking Loop system has been developed and tested. The CPLL has a bandwidth wider than 40 MHz and demonstrate an evident advantage on the RT PLL. The novel CPLL system can phase-lock more than 60% of the FFO spectral line if the free-running FFO is about 12 MHz. The integrating loop filter has been realized for the CPLL. Practical implementation of CPLL looks especially promising for phase-locking of novel superconducting local oscillators utilizing NbN / NbTiN films, as well as for interferometry applications where extremely low LO phase noise is required.

Acknowledgment

We would like to thank Pavel Yagoubov, Hans Golstein, Andrey Pankratov, Sergey Pripolzin and Vladimir Vaks for support and fruitful discussions.

References

[1] V. P. Koshelets, S. V. Shitov, L. V. Filippenko, A. M. Baryshev, H. Golstein, T. de Graauw, W. Luinge, H. Schaeffer, H. van de Stadt, "First Implementation of a Superconducting Integrated Receiver at 450 GHz" 1996 *Appl. Phys. Lett.* **68 (9)** p. 1273.

[2] V.P. Koshelets, S.V. Shitov, A.B. Ermakov, O.V. Koryukin, L.V. Filippenko, A.V. Khudchenko, M.Yu. Torgashin, P. Yagoubov, R. Hoogeveen, O.M. Pylypenko, "Superconducting Integrated Receiver for TELIS", *IEEE Trans. on Appl.Supercond.*, 2005, vol. 15, pp. 960-963.

[3] V.P. Koshelets, A.B. Ermakov, P.N. Dmitriev, A.S. Sobolev, A.M. Baryshev, P.R. Wesselius, J. Mygind, "Radiation linewidth of flux flow oscillators", *Superconductor Science and Technology*, 2001, v. 14, pp. 1040 - 1043.

[4] S. AlBanna, R. Brito, B. Shillue "ALMA 1st LO Photonic Reference: Status of Phase Drift Measurements" 2005 NRAO website. Available: http://www.tuc.nrao.edu/~bshillue/E2E_Phase_Drift_Status_RevB.doc.

[5] A.V. Khudchenko, V.P. Koshelets, P.N. Dmitriev, A.B. Ermakov, P.A. Yagoubov, and O.M. Pylypenko, "Cryogenic Phase Detector for Superconducting Integrated Receiver", *IEEE Trans. on Appl. Supercond.*, 2007, vol. 17, pp. 606-608.

[6] A.V. Khudchenko, V.P. Koshelets,, A.B. Ermakov and P.N. Dmitriev "A cryogenic phase detector for a cooled wideband phase-lock loop system", Journal of Communications Technology and Electronics, 2008, vol. 53, No. 5, pp. 594-599.

[7] A.V. Khudchenko, V.P. Koshelets, P.N. Dmitriev, A.B. Ermakov, O.M. Pylypenko, and P.A. Yagoubov, "Cryogenic Phase Locking Loop System for Flux-Flow Oscillator", Proceedings of the 19th International Symposium on Space Terahertz Technology (ISSTT-08), vol 2, pp. 511-515, 2009.