Cryogenic Phase Locking Loop System for Superconducting Integrated Receiver

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Abstract

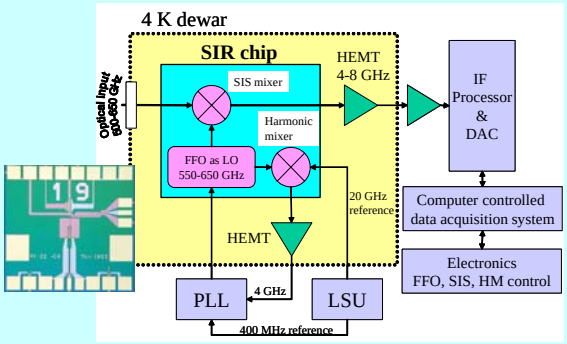
A bandwidth of the typical Phase Locking Loop (**PLL**) system for the Superconducting Integrated Receiver (**SIR**) is limited by unavoidable delays in the long cables between SIR inside cryostat semiconductor PLL system outside it. To overcome this limitation we propose Cryogenic Phase Locking Loop (**CPLL**).

A cryogenic phase detector (**CPD**) based on a superconductor-insulator-superconductor (**SIS**) junction has been proposed and preliminary tested. A sinusoidal output signal of the CPD has been measured. Experimental data demonstrate that the CPD intrinsically could operate with an effective bandwidth more than 100 MHz. The CPD is initially intended for phase locking of the Flux-Flow Oscillator (**FFO**) in the SIR.

A model describing coupling between a CPD and an FFO has been developed and experimentally verified.

A design of the CPLL system for the SIR is presented. An effective bandwidth of the CPLL system exceeds 25 MHz at an operation frequency of 400 MHz. This is considerably better than bandwidth of the room-temperature PLL system which is limited to 12 MHz. The novel CPLL system synchronizes 50% of the FFO power for free-running FFO linewidth of about 10 MHz, compare to 20% in the case of regular PLL system. It results in improvement of the FFO spectral ratio and would expand the SIR operation range.

Superconducting Integrated Receiver

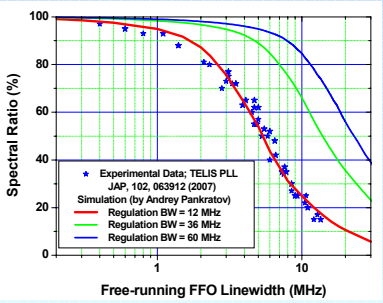


Schematics of the FFO stabilization circuit. FFO frequency is mixed in HM with the 19-21 GHz reference. The mixing product is amplified, downconverted and compared with the 400 MHz reference in the PLL. The phase difference signal generated by PLL is used to feedback the FFO control line.

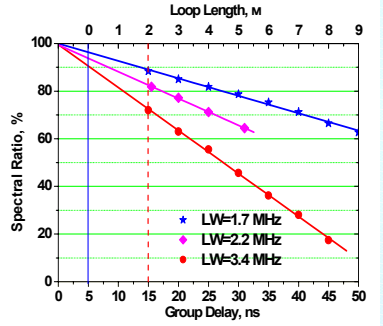
Ultrawideband PLL is required (>50 MHz):

For the future SIR applications (f>1THz) an FFO with the NbN electrodes will be used; the FFO linewidth could considerably exceed 10 MHz.

The specification for a ALMA interferometer require a phase stability better then 75 fs. To realise such a stability for the SIR a part of phase locked FFO power – **Spectral Ratio (SR),** as hight as 90% is needed.

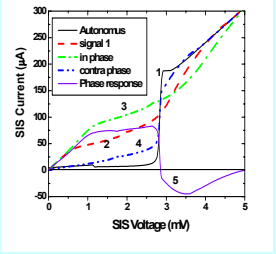


The Dependence of the SR vs FFO linewidth for different PLL bandwidths.

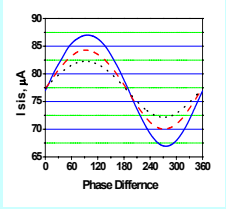


The PLL bandwidth is determined by a total group delay in the loop. A bandwidth of the typical PLL system for the SIR is limited by unavoidable delays in the long cables between the SIR inside a cryostat and semiconductor PLL system outside it. To overcome this limitation we propose the CPLL.

SIS - Cryogenic Phase Detector for the CPLL

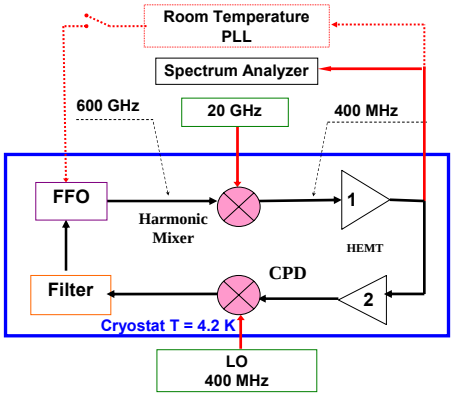


I-VCs of a SIS junction. Microwave signals (5 GHz) are applied.



A SIS is a well known mixer element. Sinusoidal response of SIS in dependence on phase difference between coming microwave signals demonstrate it can be a CPD. The CPD could operate with effective bandwidth more than 100 MHz.

Concept of the Cryogenic PLL



All the elements of the Cryogenic PL Loop are inside the cryostat with a FFO. It allows to minimize the loop length and the time delay.

Experimental realization of the CPLL

	Loop length(м)	Delay in elements(ns)	Total Delay(ns)	Bandwidth(MHz)
CryoPLL	1	2	15	27
RoomPLL	2	5	7	12

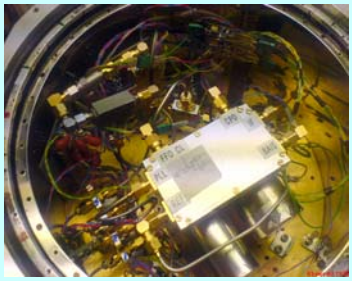
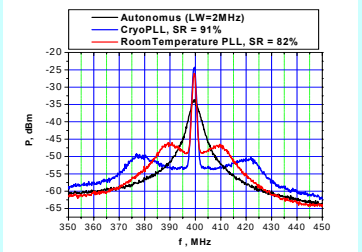
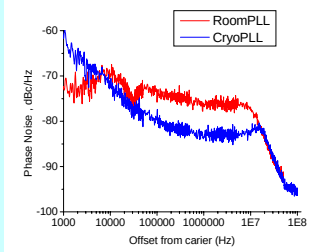


Photo of the CPLL in cryostat. FFO and CPD are placed in two separated shields. Length of the loop is 1m.



Downconverted spectra of FFO. The demonstration of CPLL advantage - for linewidth 2 MHz it gives SR = 91% as contrasted with 82% for the Room Temperature PLL system.



The CPLL demonstrate a better Phase Noise then the Room Temperature PLL at frequencies more then 10kHz .

Summary

- A new and successful application of a SIS junction - cryogenic phase detector (CPD).
- The CPD intrinsically could operate with an effective bandwidth more than 100 MHz. The maximal output signal is about 0.1 mV.
- A concept of CryoPLL system has been proven. Bandwidth as wide as 27 MHz has been obtained in the first experiments.
- The improvement of the phase locked FFO spectral ration from 20% to 50% has been achieved at application of the CryoPLL for FFO linewidth 10 MHz.
- Practical application of the CPD looks especially promising for the development of SIR arrays.
- The first CryoPLL system with operation frequency 4 GHz has been successfully tested.

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