Superconducting Integrated Submillimeter Receiver for TELIS

Valery Koshelets, Andrey Ermakov,
Lyudmila Filippenko, Andrey Khudchenko, Oleg Kiselev,
Alexander Sobolev, Mikhail Torgashin,
Institute of Radio Engineering and Electronics (IREE), Moscow, Russia

Pavel Yagoubov, Ruud Hoogeveen, and Wolfgang Wild
SRON Netherlands Institute for Space Research, the Netherlands

Superconducting Integrated Receiver (SIR) for TELIS

Outline

- TELIS project; SIR channel
- SIR chip design and performance:
  - Chip Layout; FFO Optimization,
  - Noise Temperature,
  - Beam Pattern,
  - IF Performance,
  - Spectral Resolution,
  - Remote Control
- Nb-AlN-NbN SIR – first implementation
- Conclusion

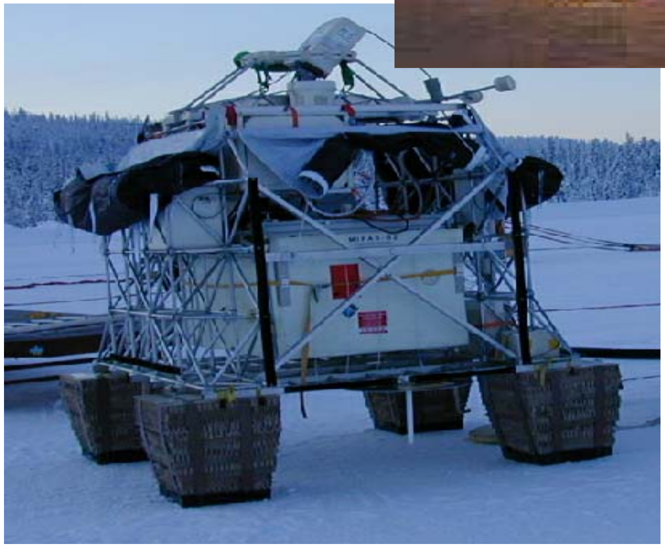
TELIS - TErahertz LImb Sounder

TELIS Objectives:

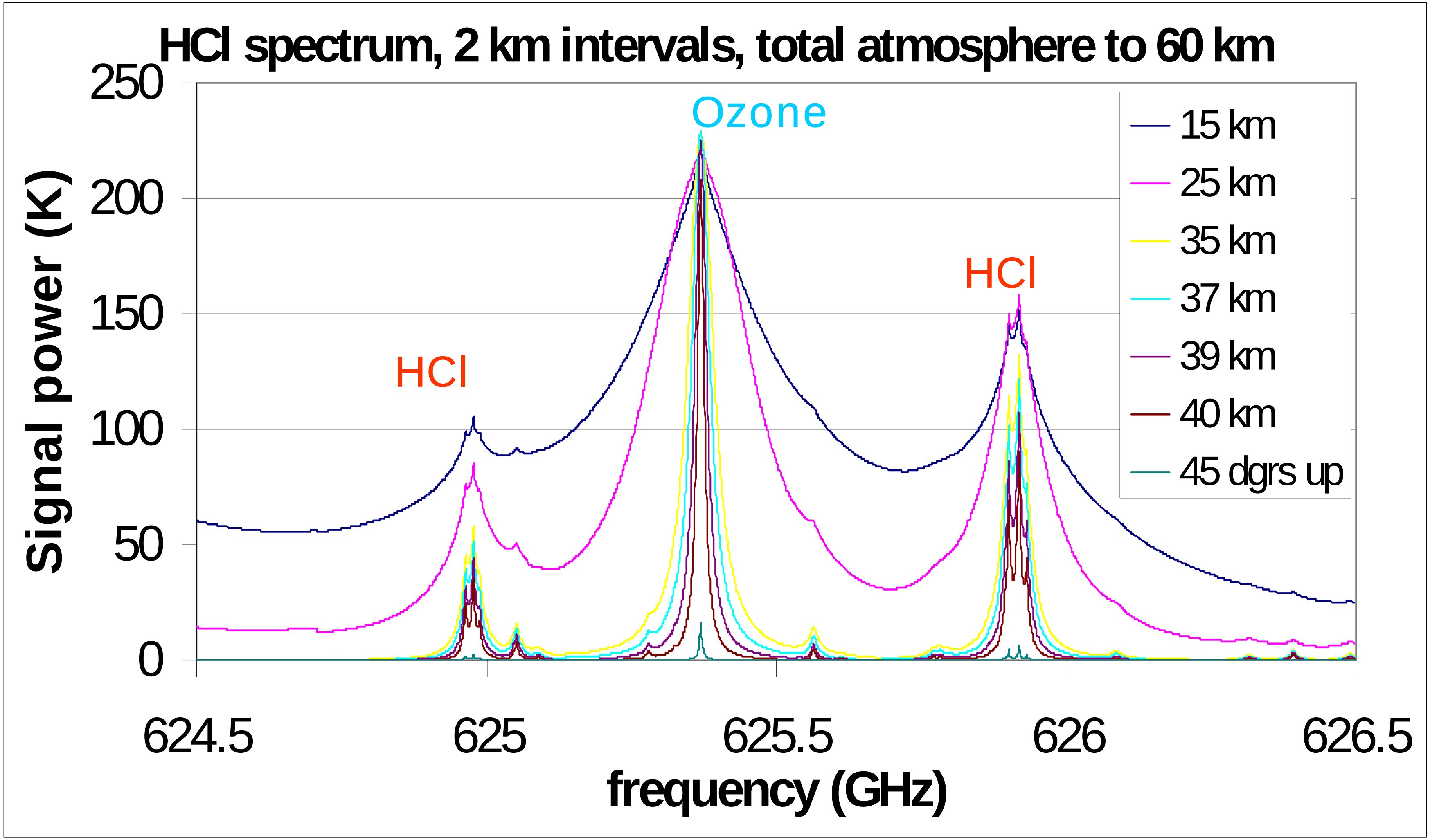
- Measure many species for atmospheric science (ClO, BrO, O_3, HCl, HOCl, etc);
  - Chemistry, Transport, Climate
- Serve as a test platform for new sensors
- Serve as validation tool for future satellite missions

Three independent frequency channels, cryogenic heterodyne receivers:

- 500 GHz by RAL
- **600-650 GHz by SRON-IREE**
- 1.8 THz by DLR (PI)



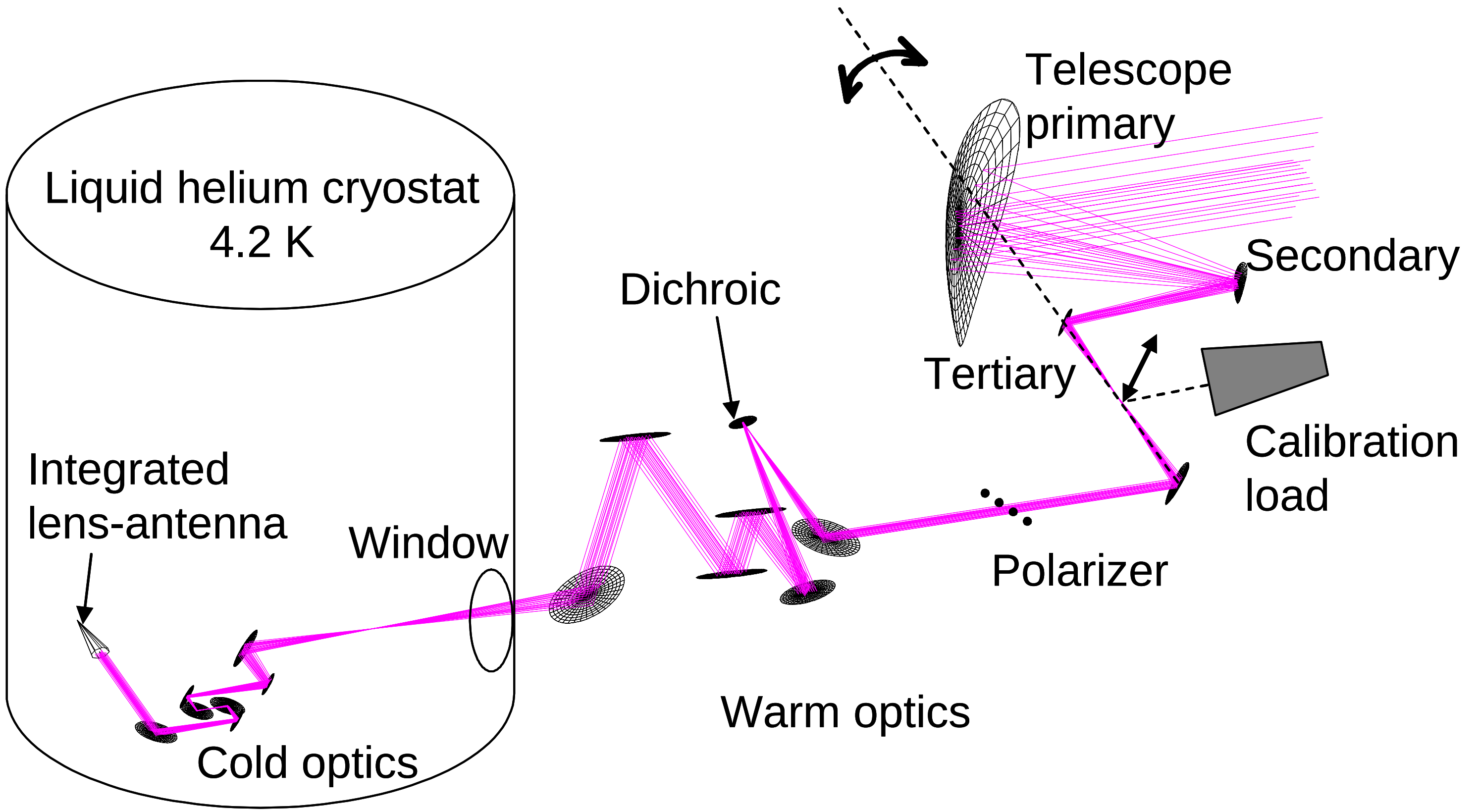
Simulated spectra for Ozone and HCl at 625 GHz



TELIS-SIR Main Parameters

##	Description	Value
1	**Input frequency range, GHz (Base line)**	**600 – 650**
2	**Input frequency range, GHz (Goal)**	**550 – 650**
3	**Minimum noise temperature in the range (DSB), K**	**250**
4	**Output IF range, GHz**	**4 - 8**
5	**Spectral resolution (width of the spectral channel), MHz**	**1**
6	**Contribution to the nearest spectral channel by phased locked FFO (dynamic range of the spectrometer), dB**	**-20**
7	**Contribution to a spectral channel by phased locked FFO at 4-6 GHz offset from the carrier, K**	**20**
8	**LO frequency net (distance between nearest settings of the PL FFO frequency), MHz**	**< 300**
9	**Dissipated power at 4.2 K stage (including IF amplifiers chain), mW**	**100**
10	**Operation temperature, K**	**< 4.5**

Schematics of the 550-650 GHz channel optics.



Wire grid polarizer and dichroic plate are used to separate this receiver from the two other frequency channels (not shown). The cold optics and mixer element are located inside the cryostat at the ambient temperature 4.2 K

Layout of SIR cold channel

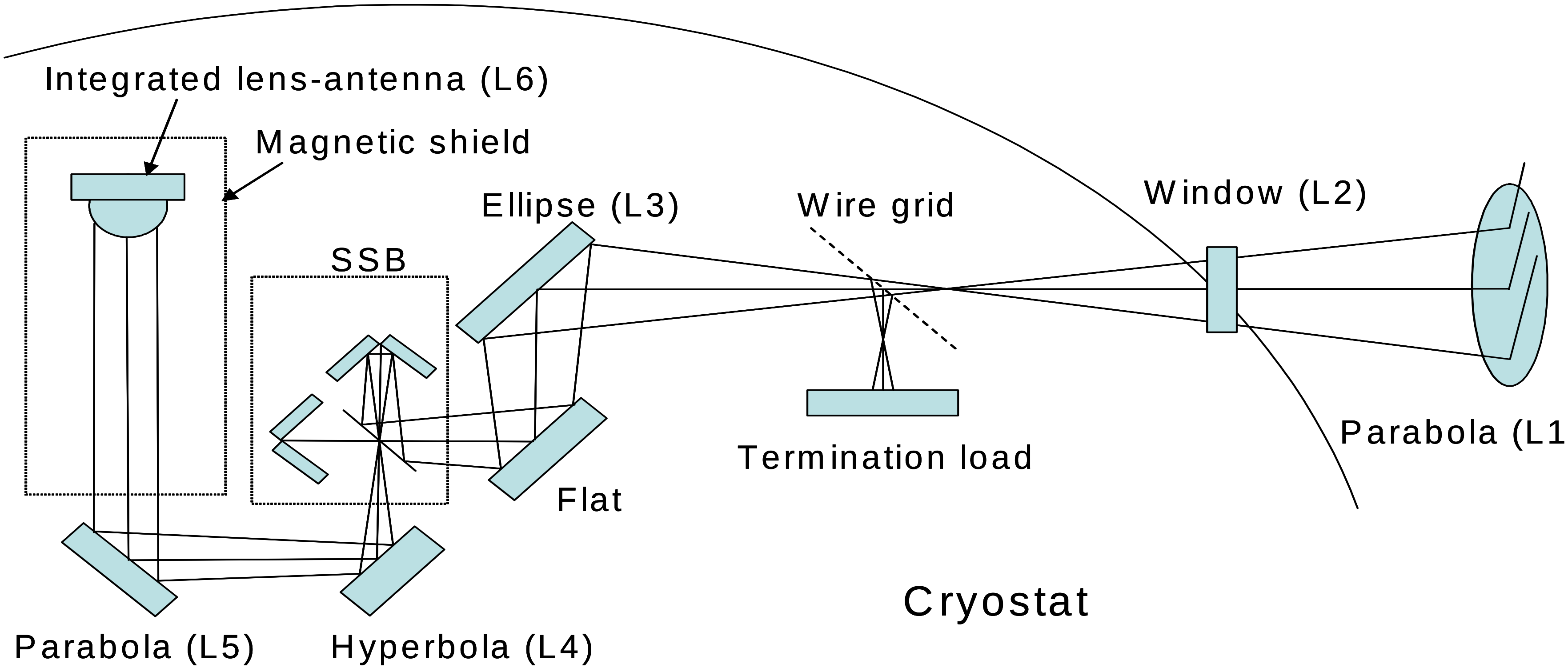
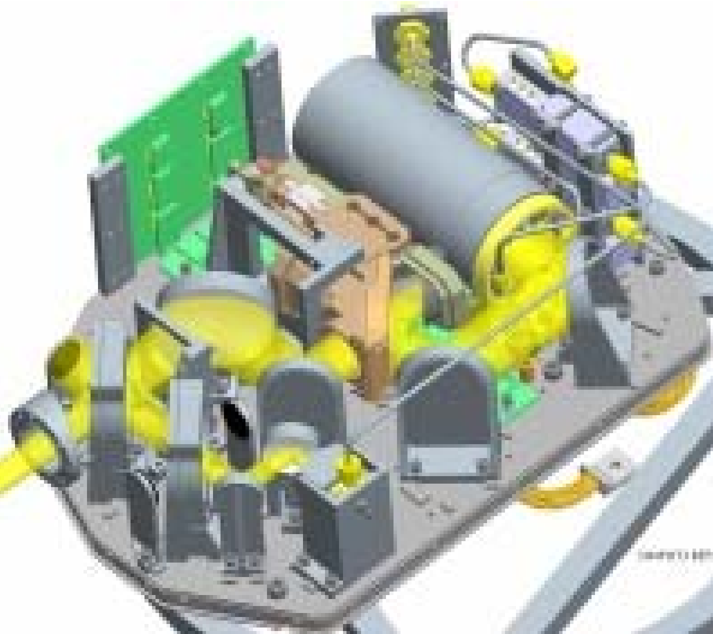
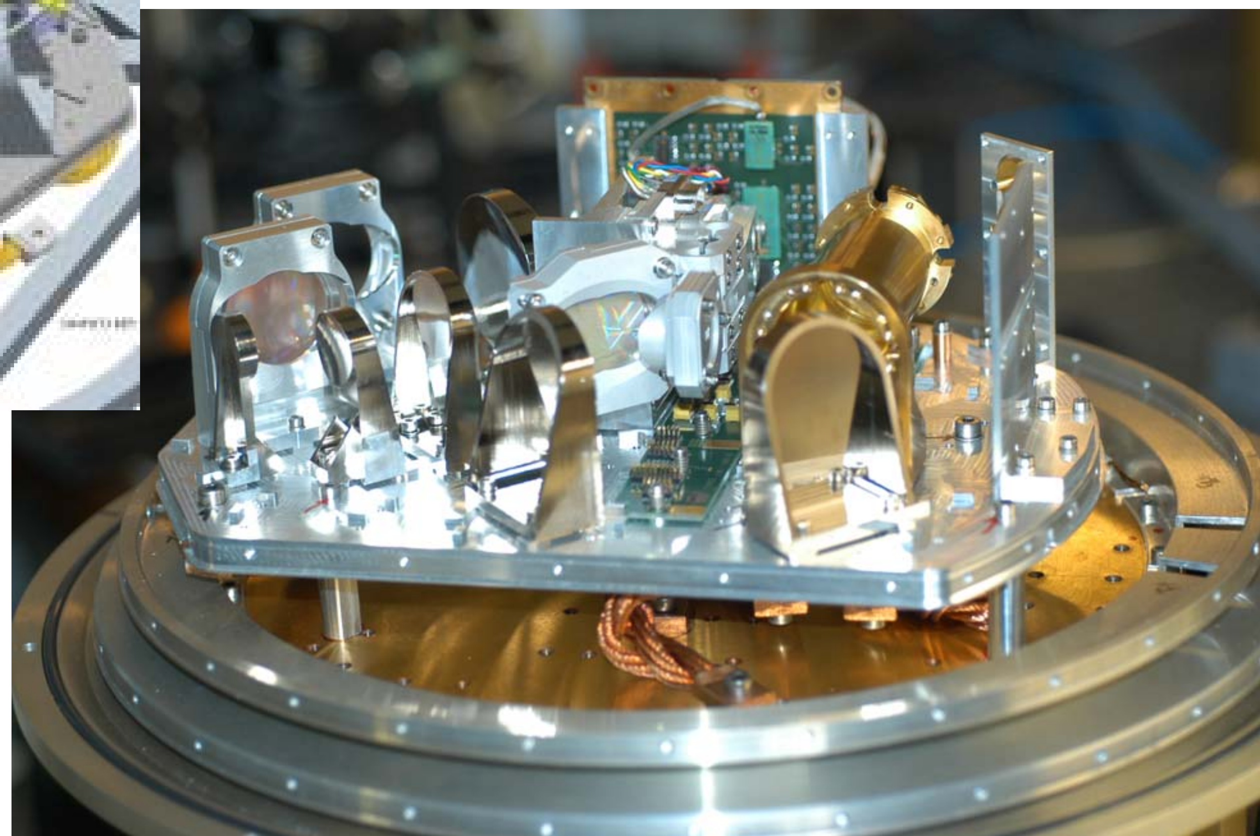
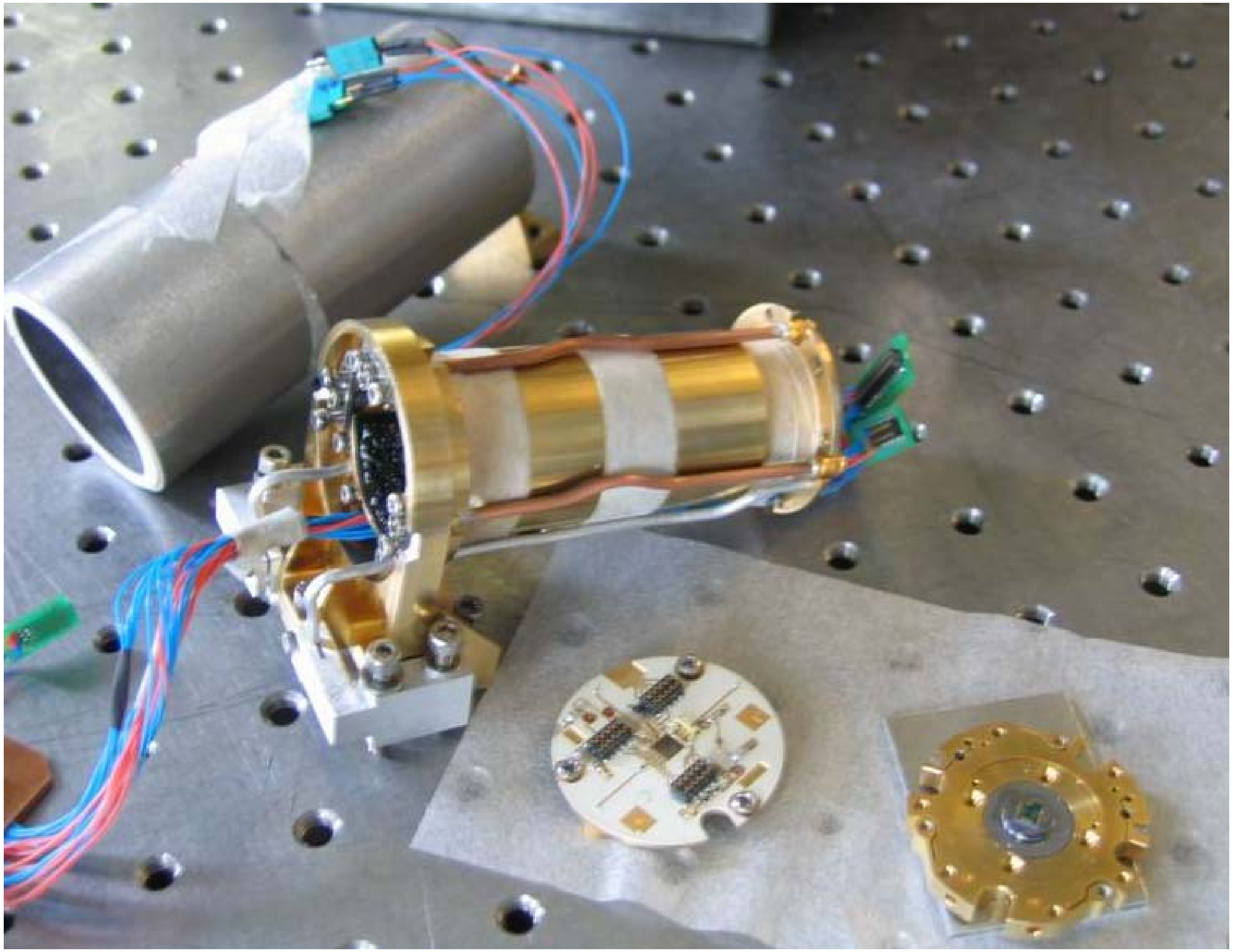


Photo of the SIR-TELIS channel





SIR Mixer Block with Shields



Schematics of PLL SIR

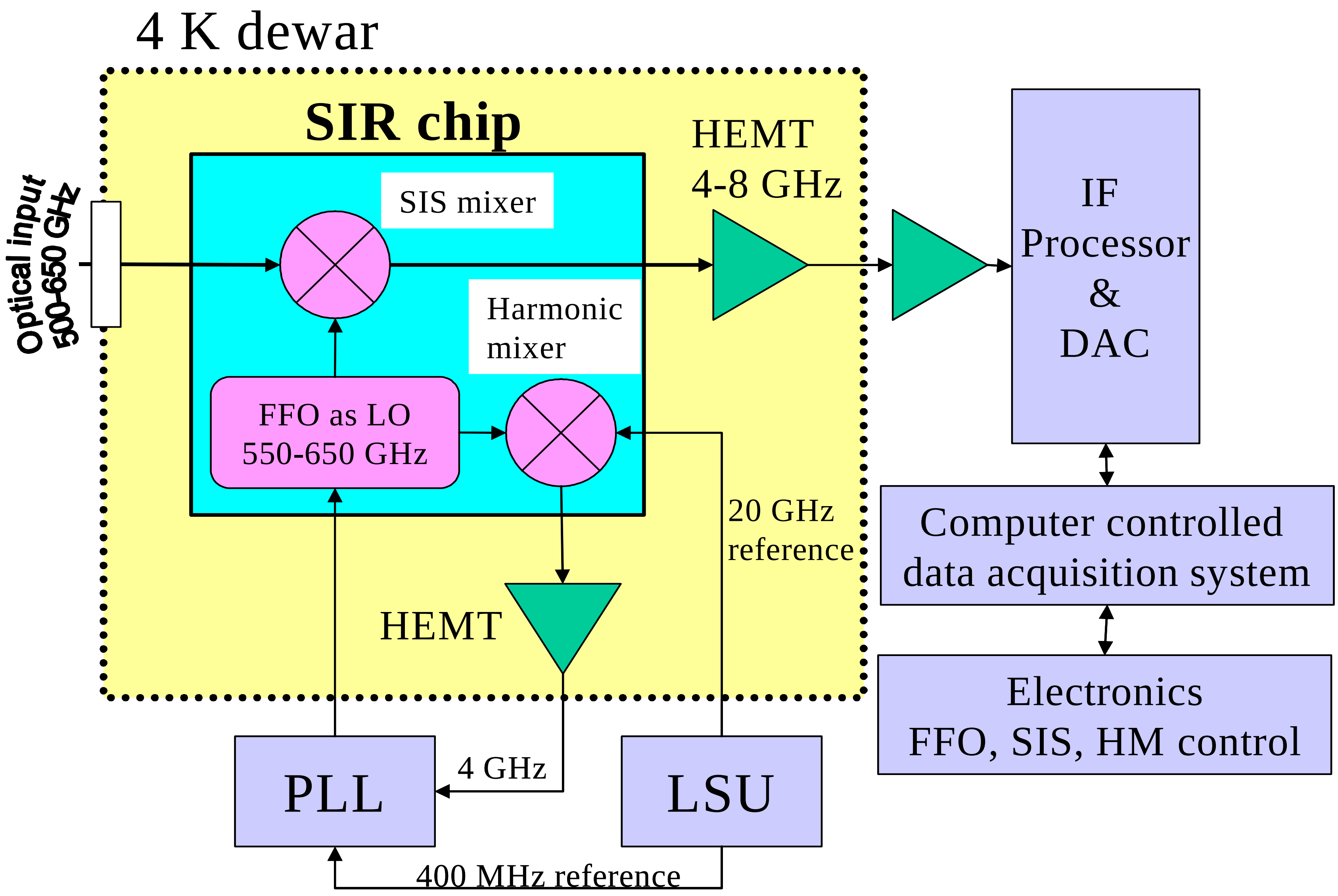
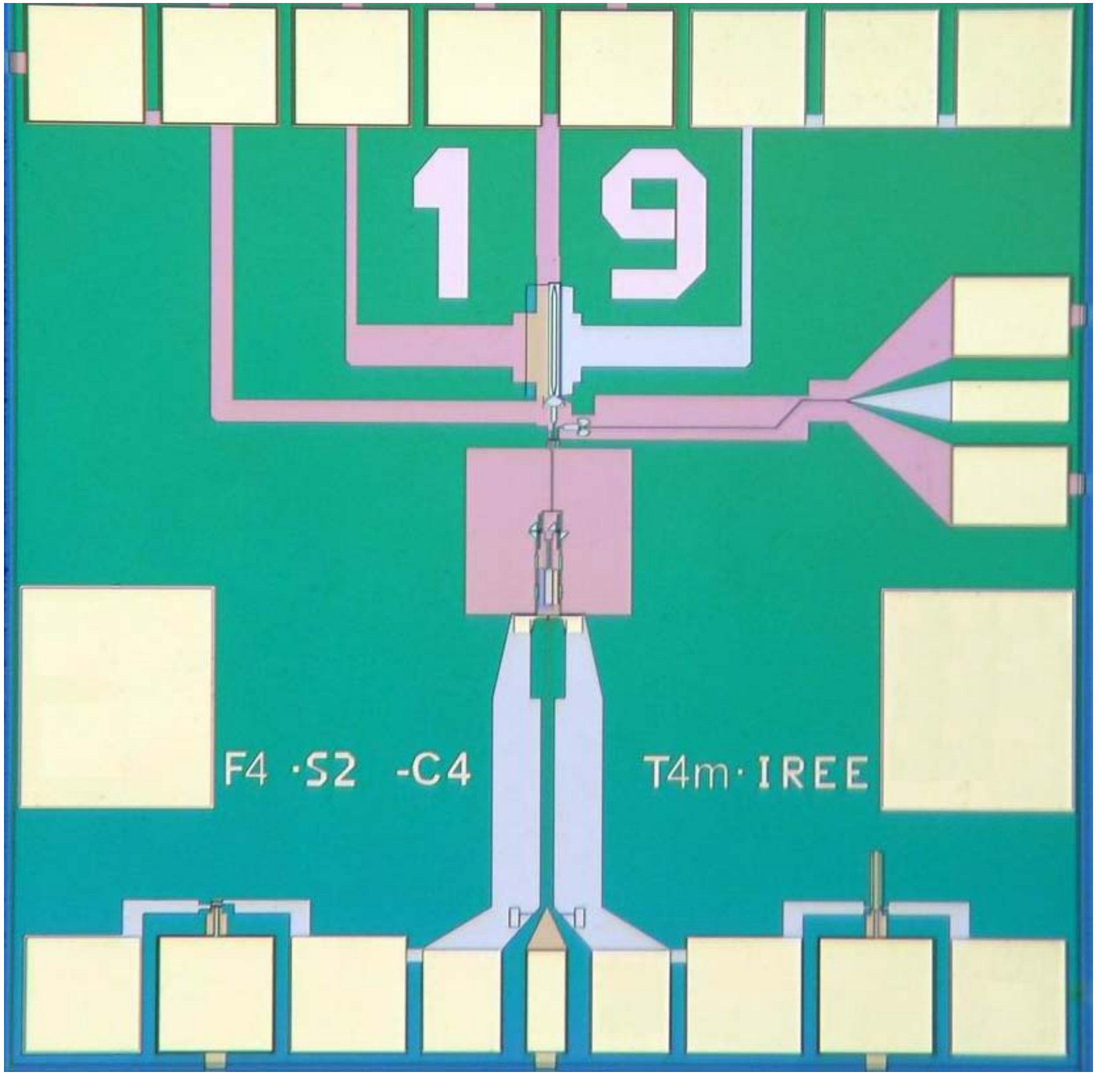
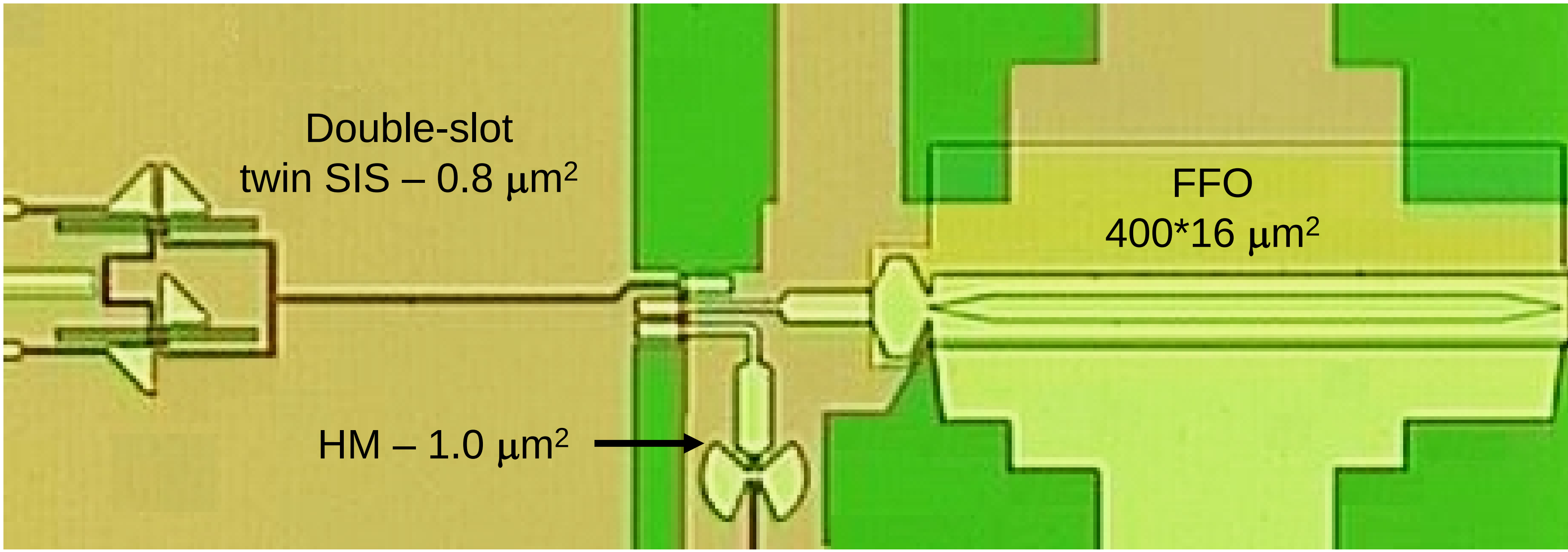


Photo of the T4m SIR chip



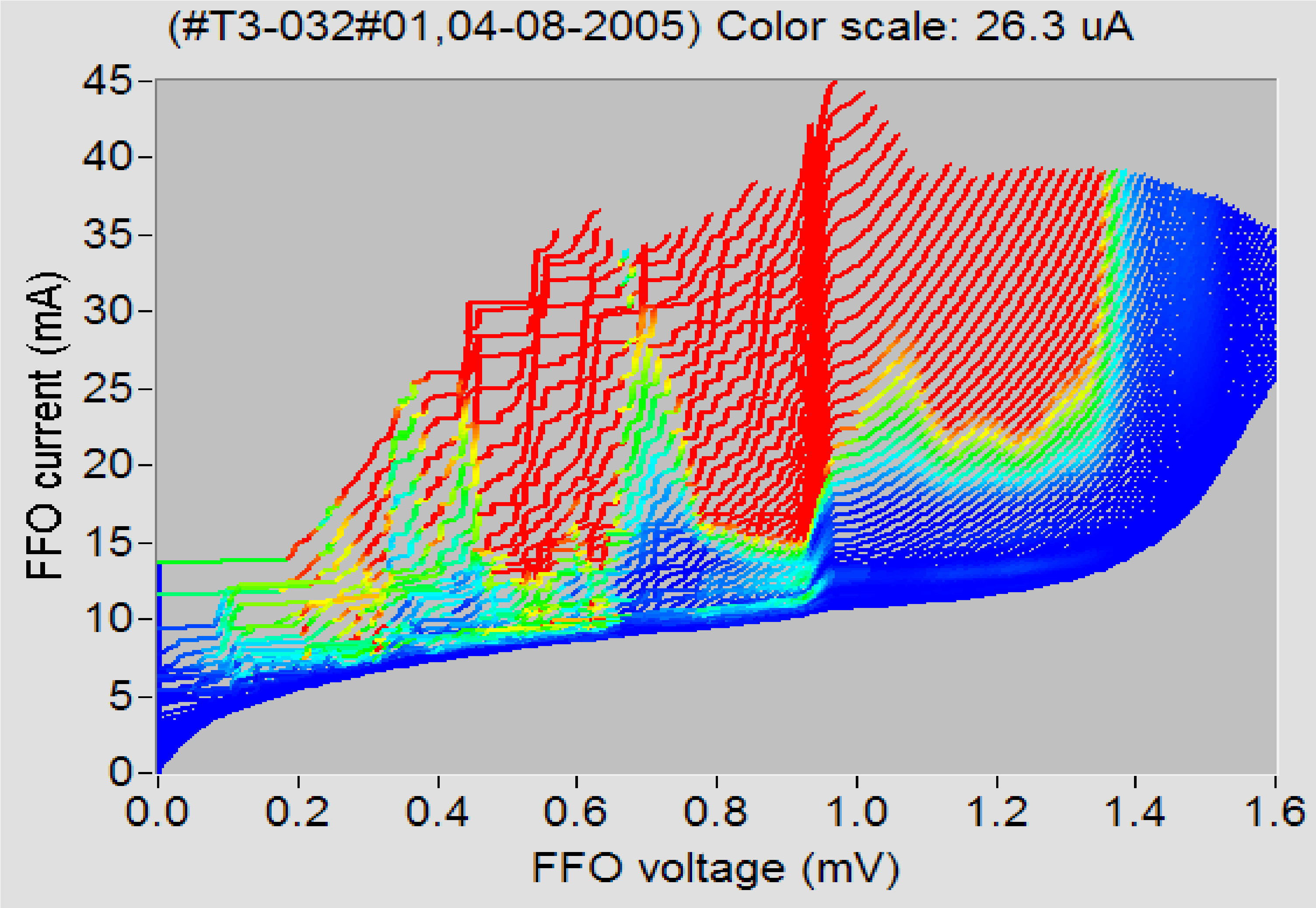
SIR Microcircuit for TELIS



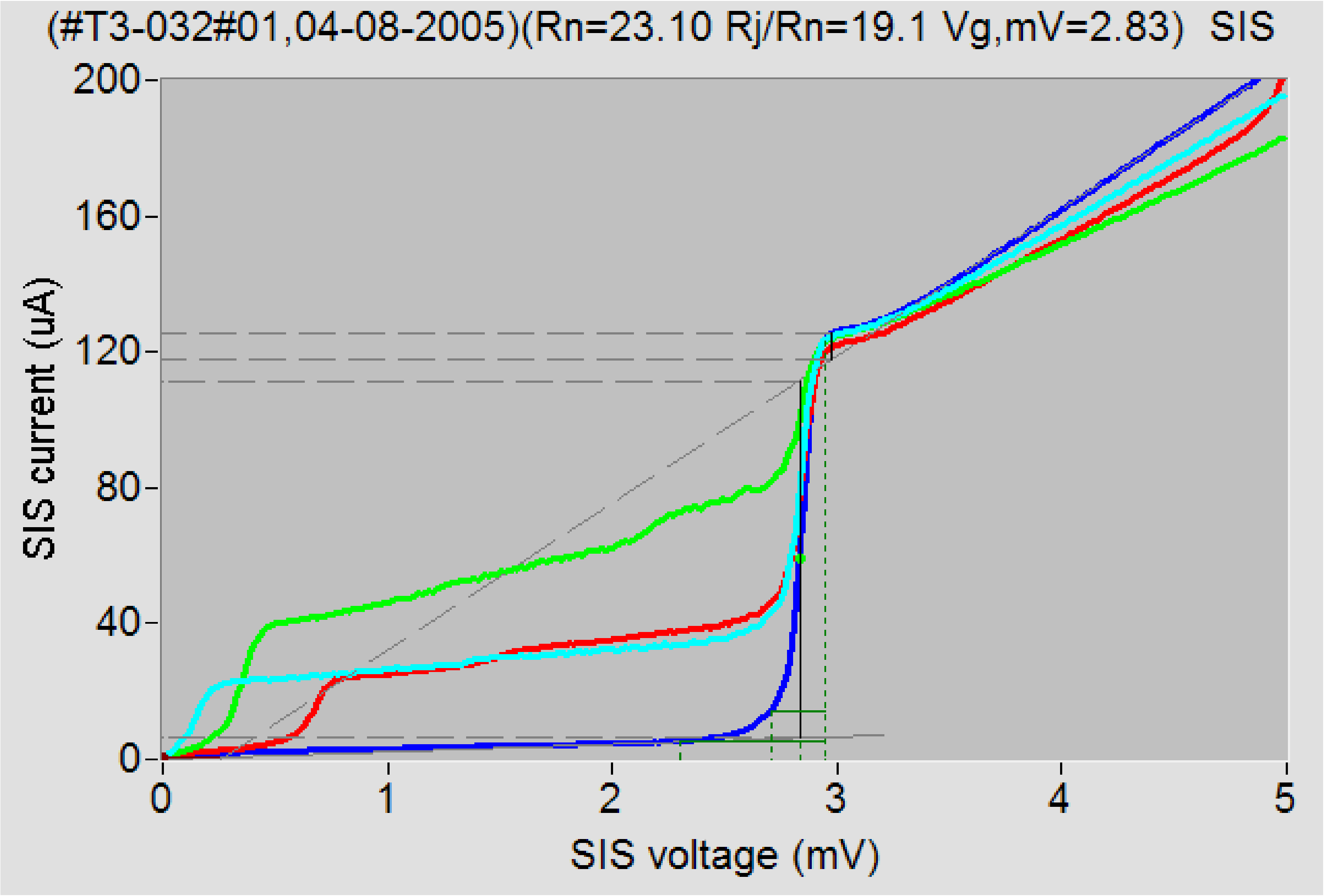
4 x 4 x 0.5 mm^3 (Si); Nb-AlOx-Nb; Jc = 5 - 8 kA/cm^2

Optionally: SIS – Jc = 8 kA/cm^2; FFO + HM = 4 kA/cm^2

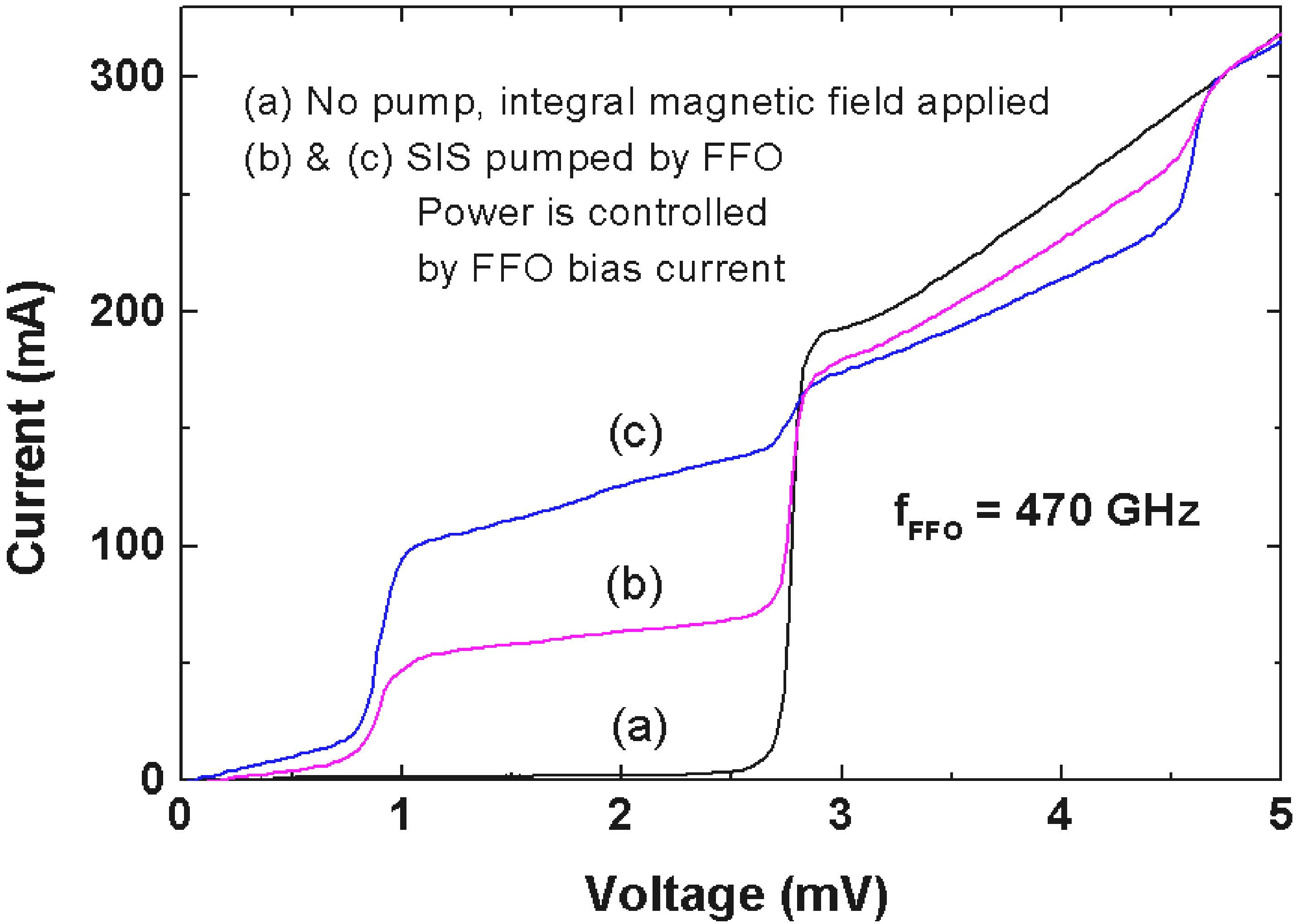
IVCs of the FFO of T3 design measured at different CL currents (red = > 25% of SIS Ig)



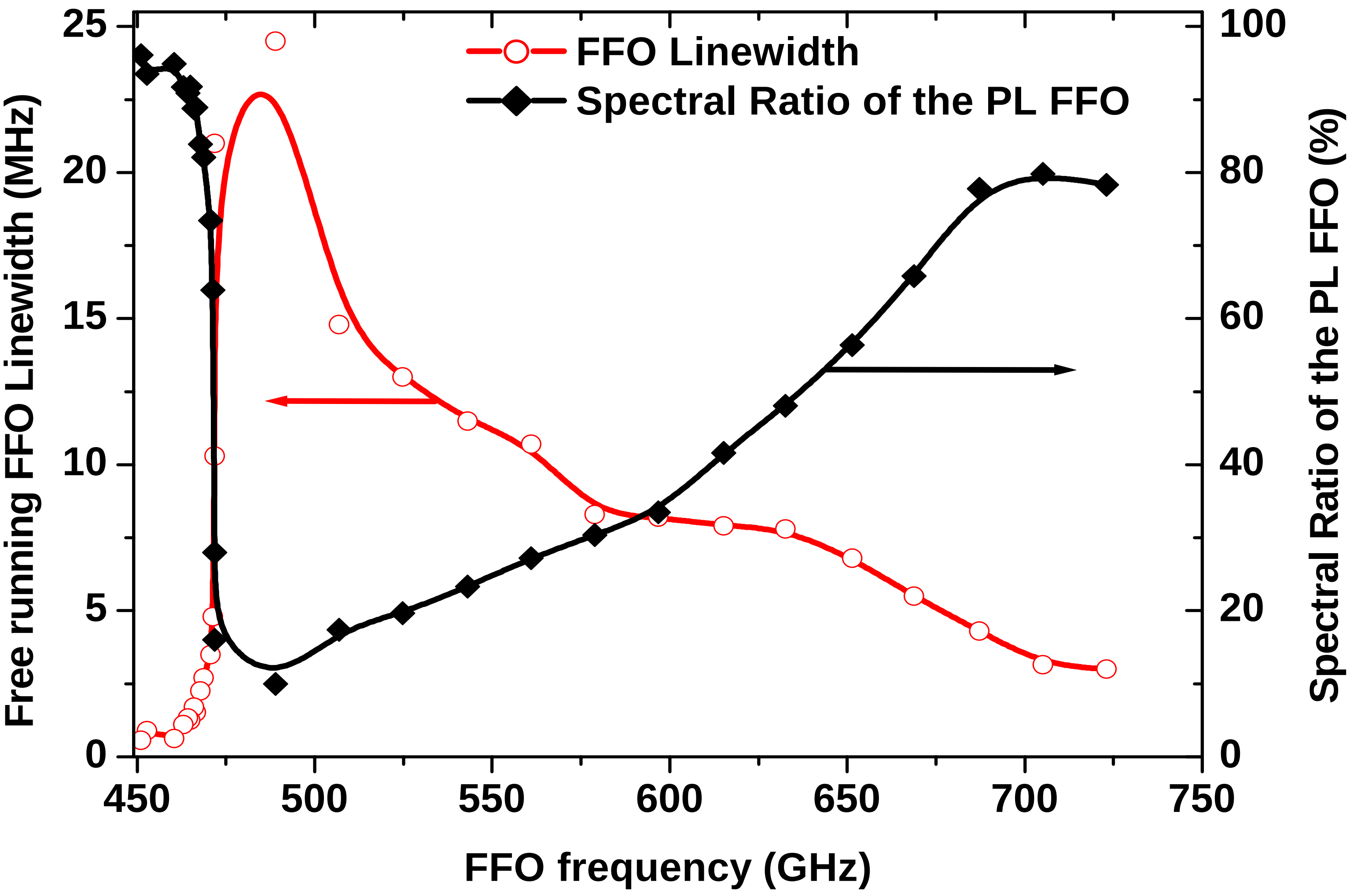
IVCs of the SIS-mixer of T3 design; f FFO = 522, 600 and 650 GHz



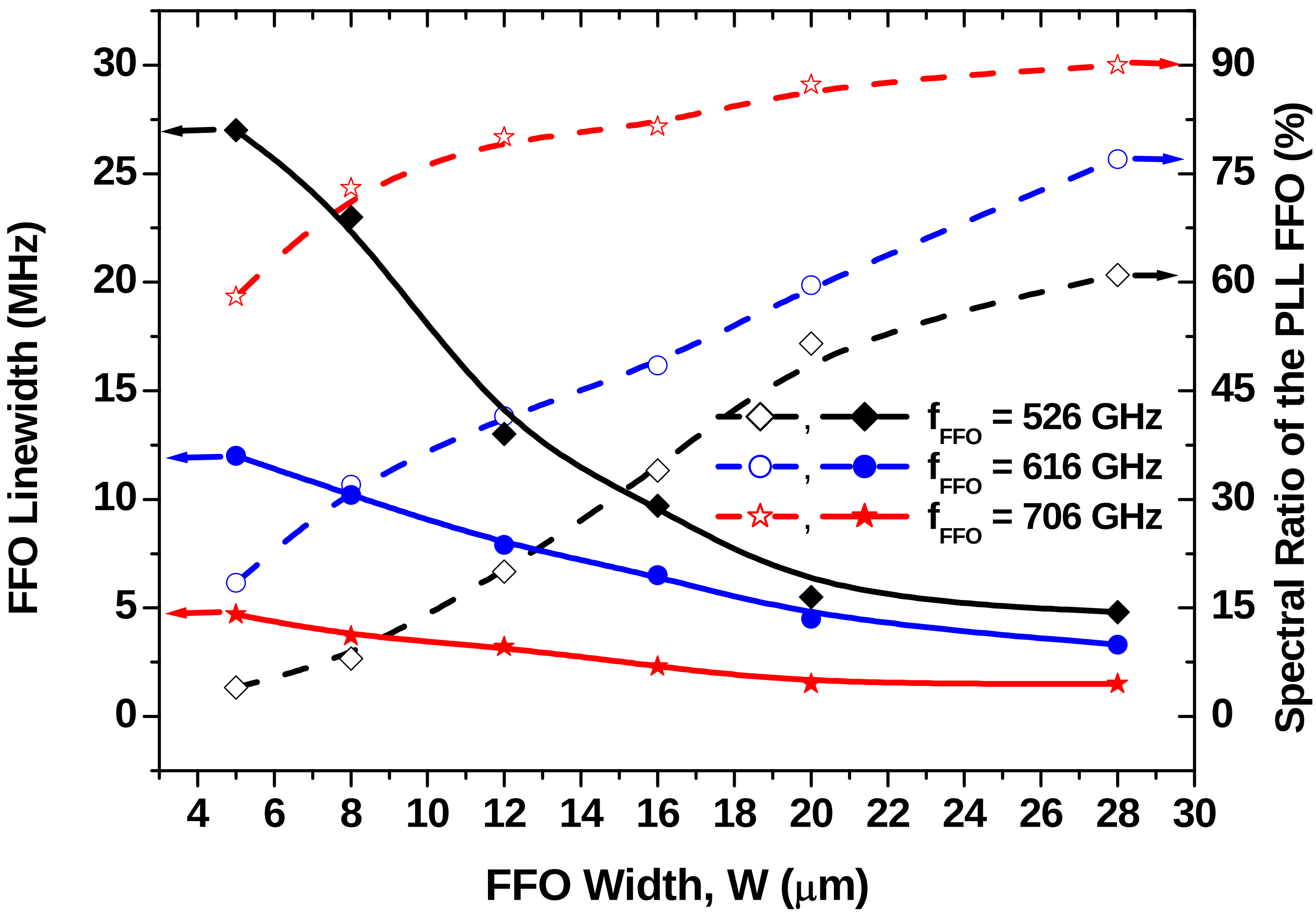
FFO + SIS; Power Control



FFO linewidth and Spectral Ratio PL FFO on its oscillation frequency.

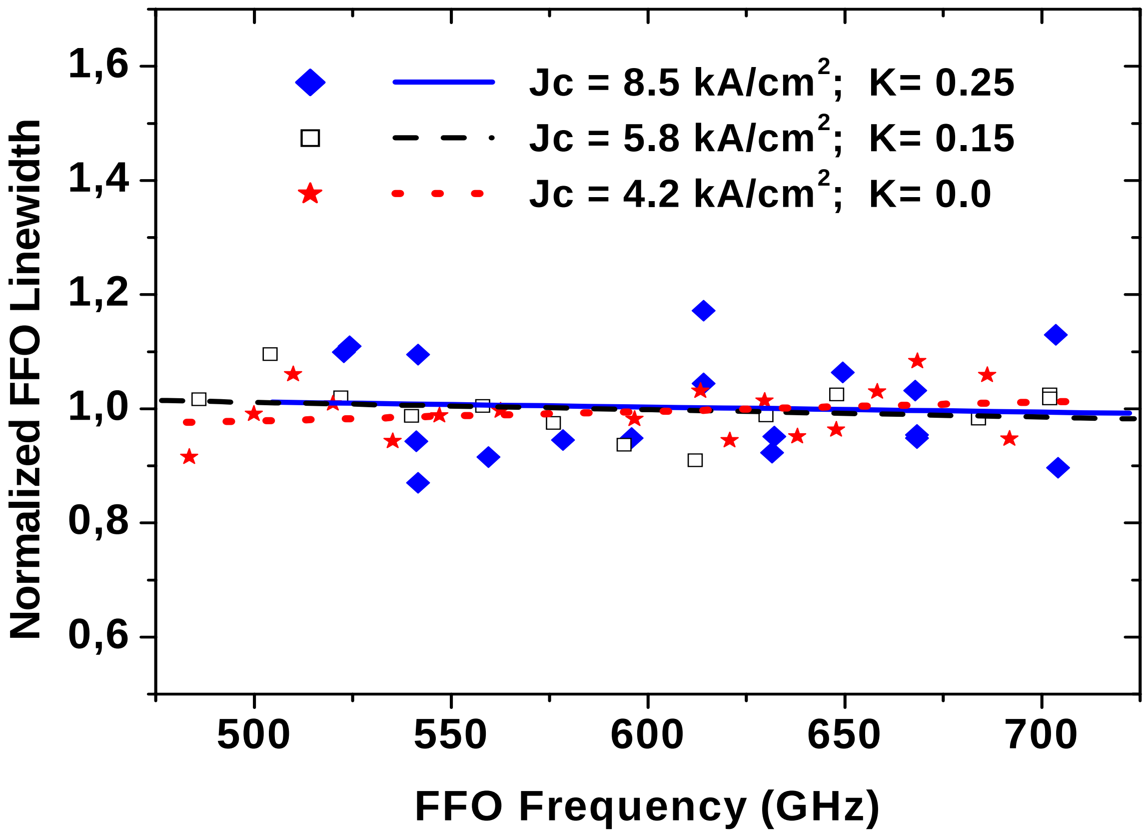


Linewidth of free-running FFOs and SR for the PL FFO as a function of FFO width (RnS =30 Ω*μm²)

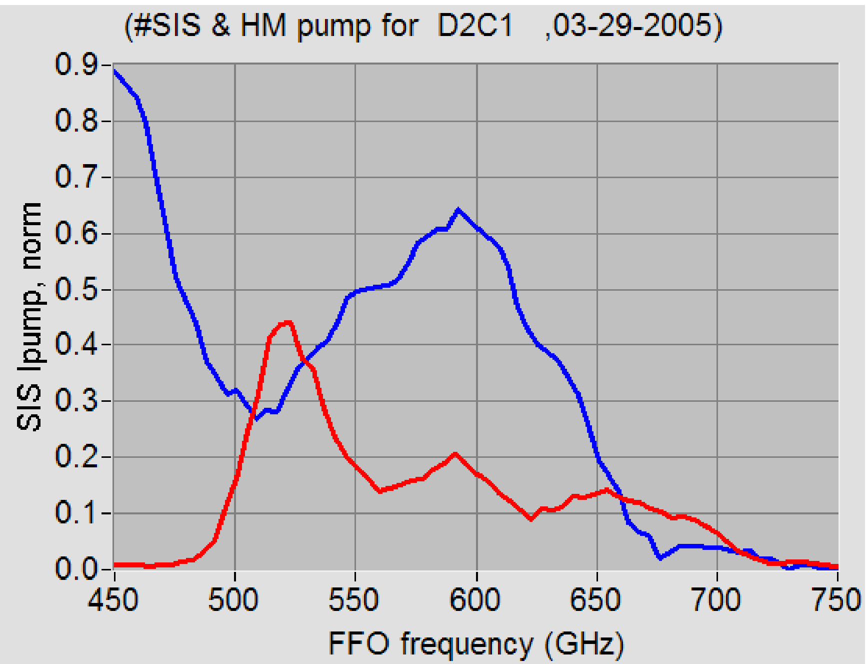


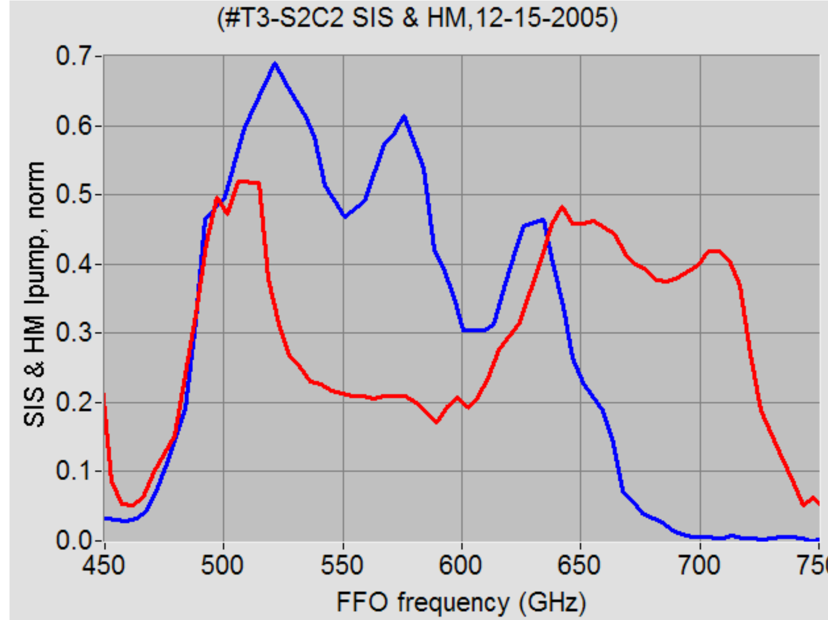
Normalized FFO Linewidth

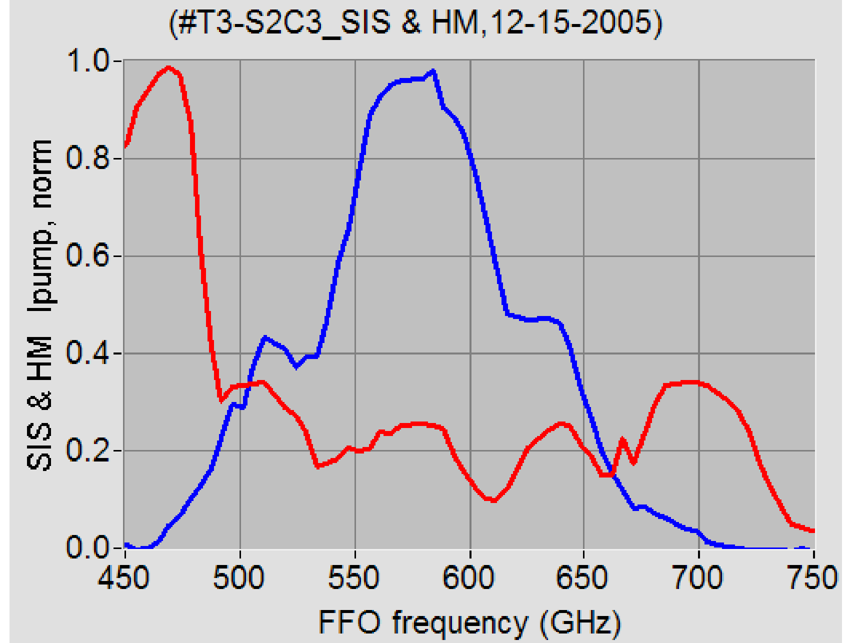
$$\Delta f := \left(\frac{2\cdot e}{h}\right)^2 \cdot \left(R_d + K\cdot R_{dCL}\right)^2 \cdot \left[\frac{e\cdot(Iqp)}{2\cdot\pi}\cdot \coth\left(\frac{e\cdot V}{2\cdot k_b\cdot T}\right) + \frac{2\cdot e\cdot(Is)}{2\cdot\pi}\cdot \coth\left(\frac{e\cdot V}{k_b\cdot T}\right)\right] + \frac{1}{\pi}\cdot\left(\frac{2\cdot e}{h}\right)\cdot\left(R_d + R_{dCL}\right)\cdot I_{lf}$$



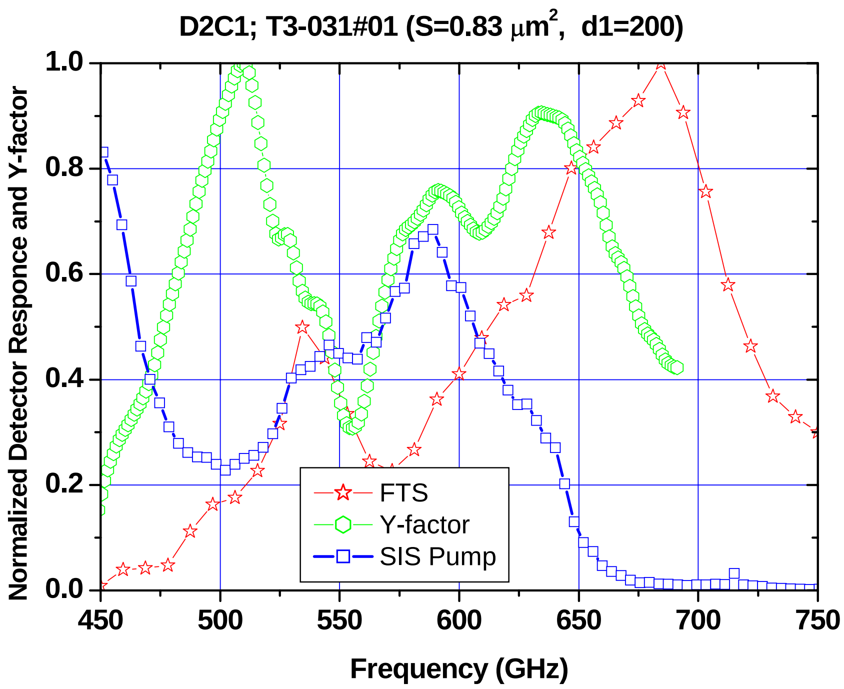
Averaged SIS (blue) and HM (red) pump for different T3 SIRs

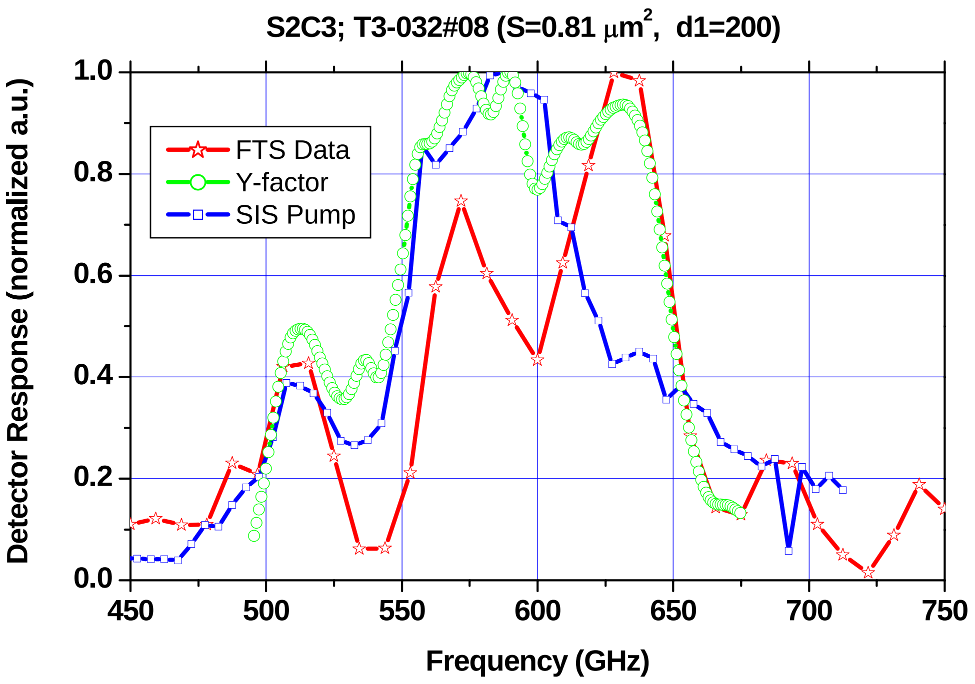




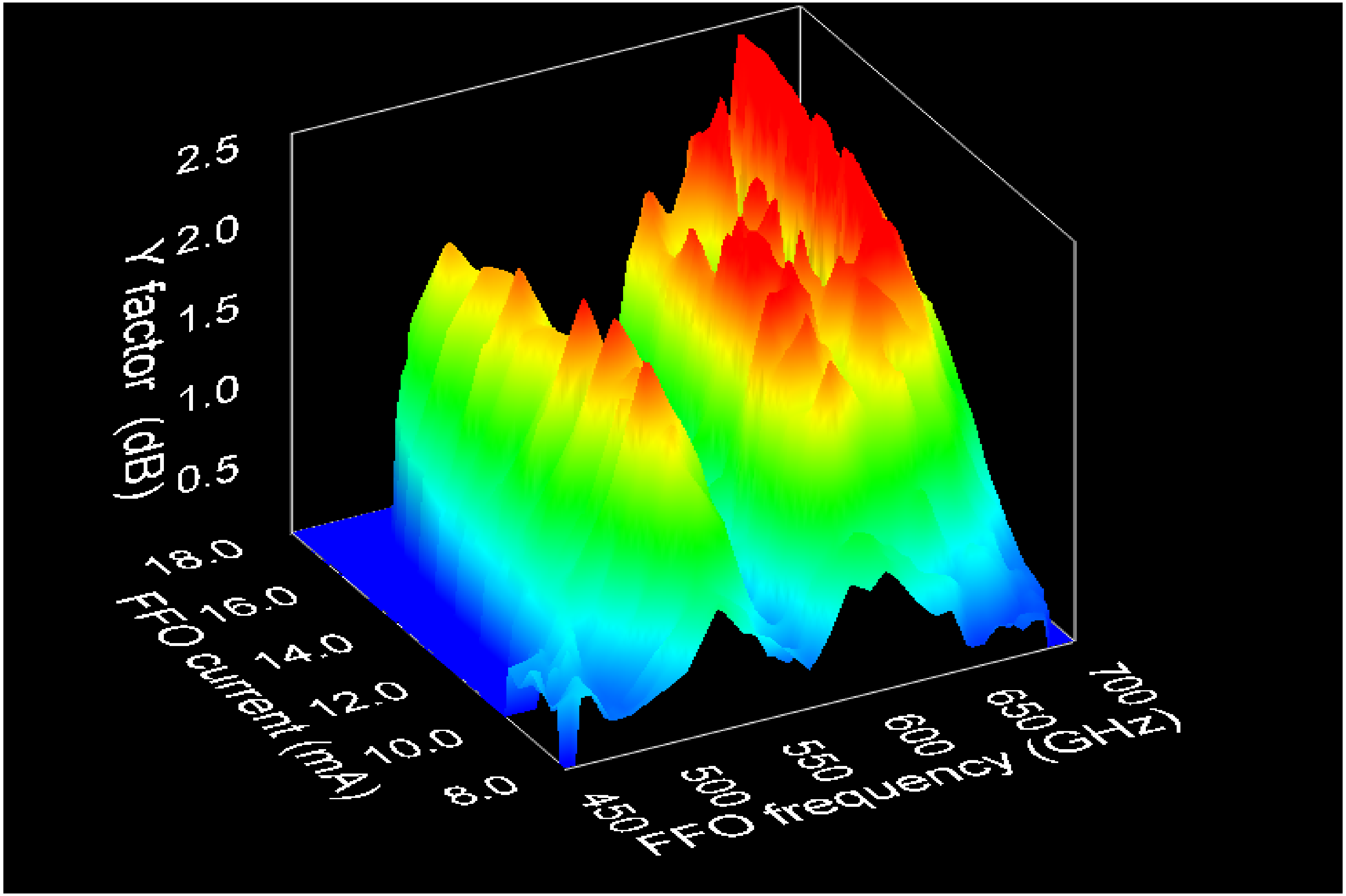


Comparison of the FTS data, Y factor and SIS pump for T3 SIRs

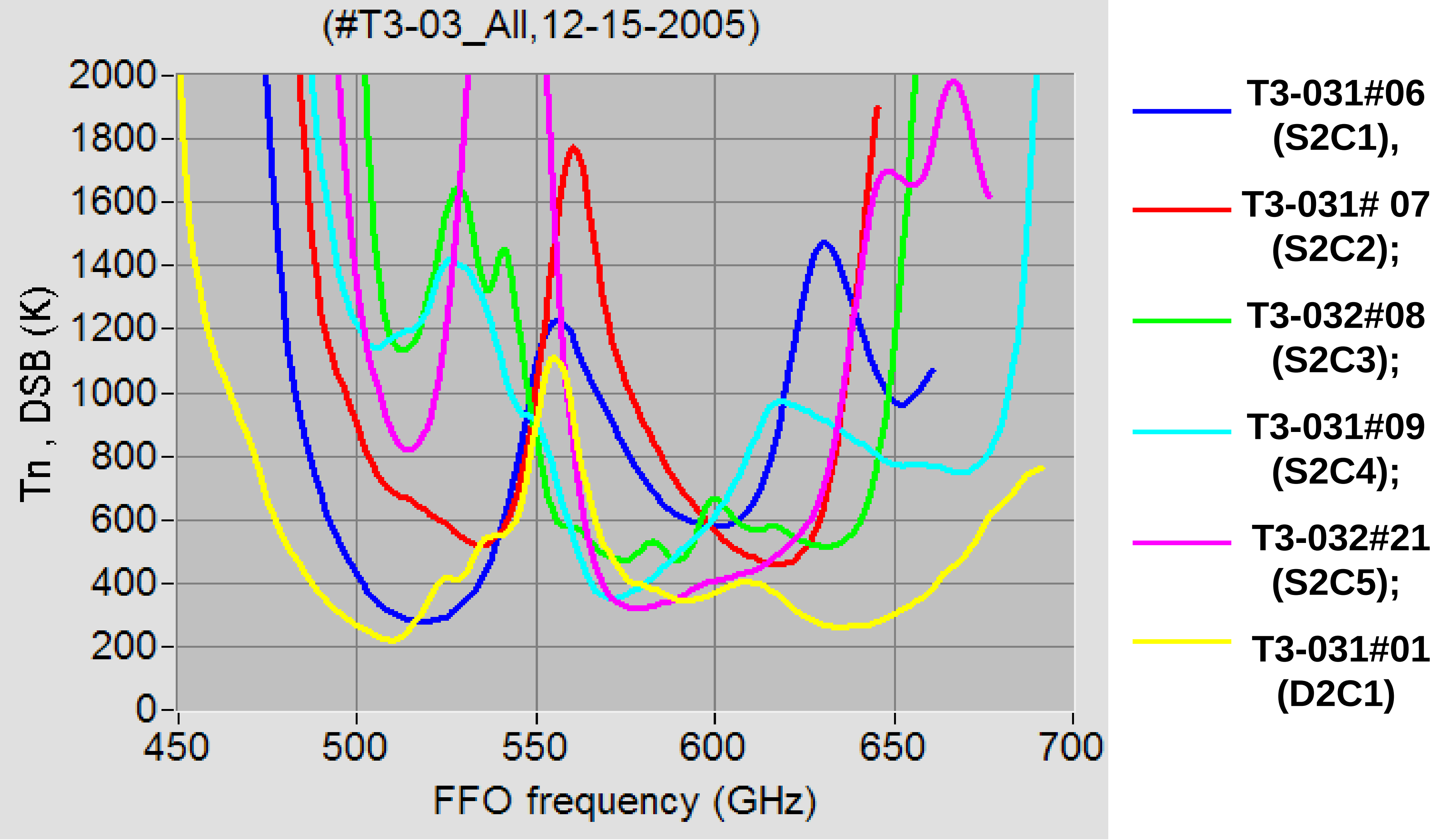




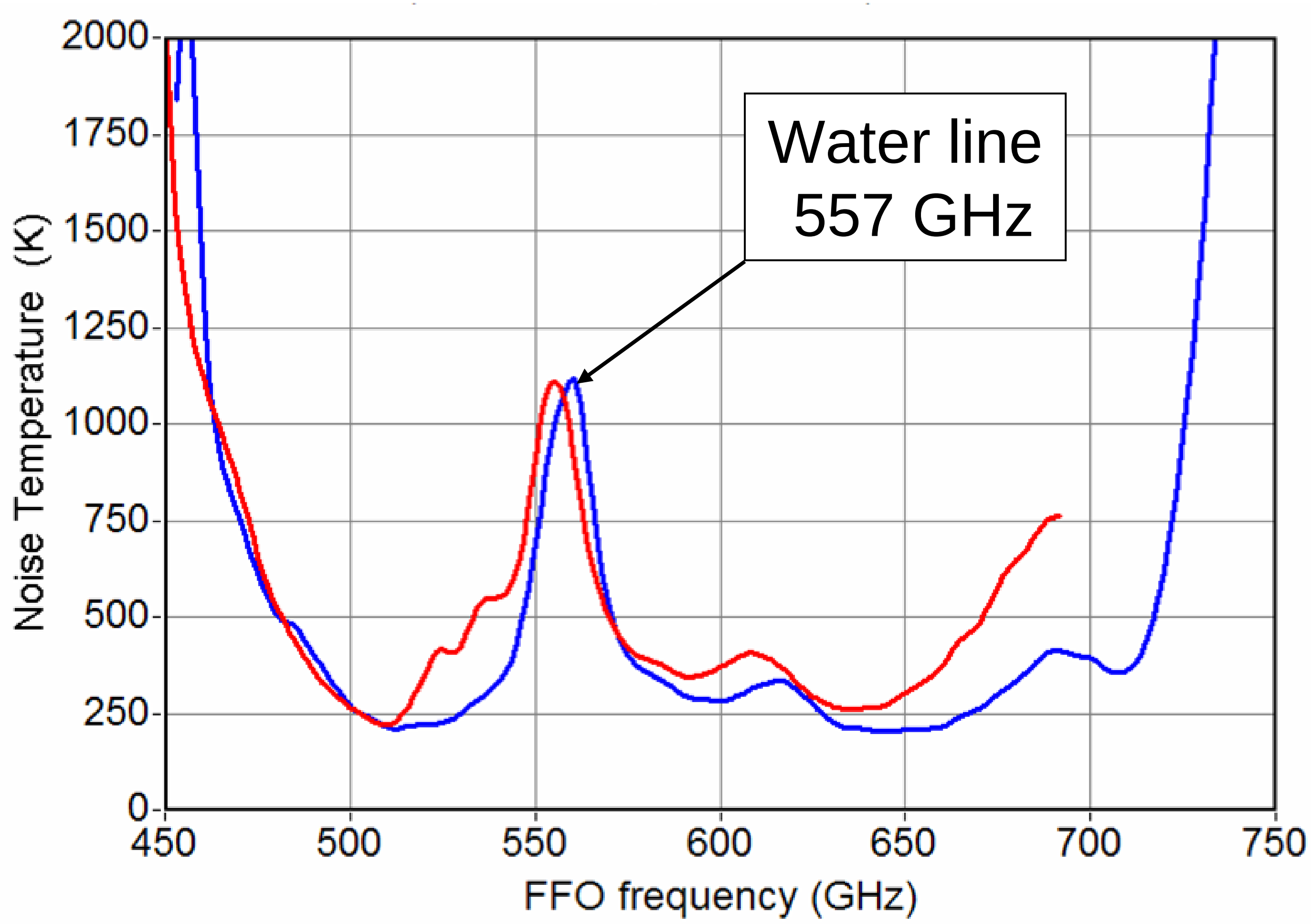
Y-factor of the SIR,
T= 2.1 K, V_{SIS} = 2.2 mV, IF = 4.3 GHz



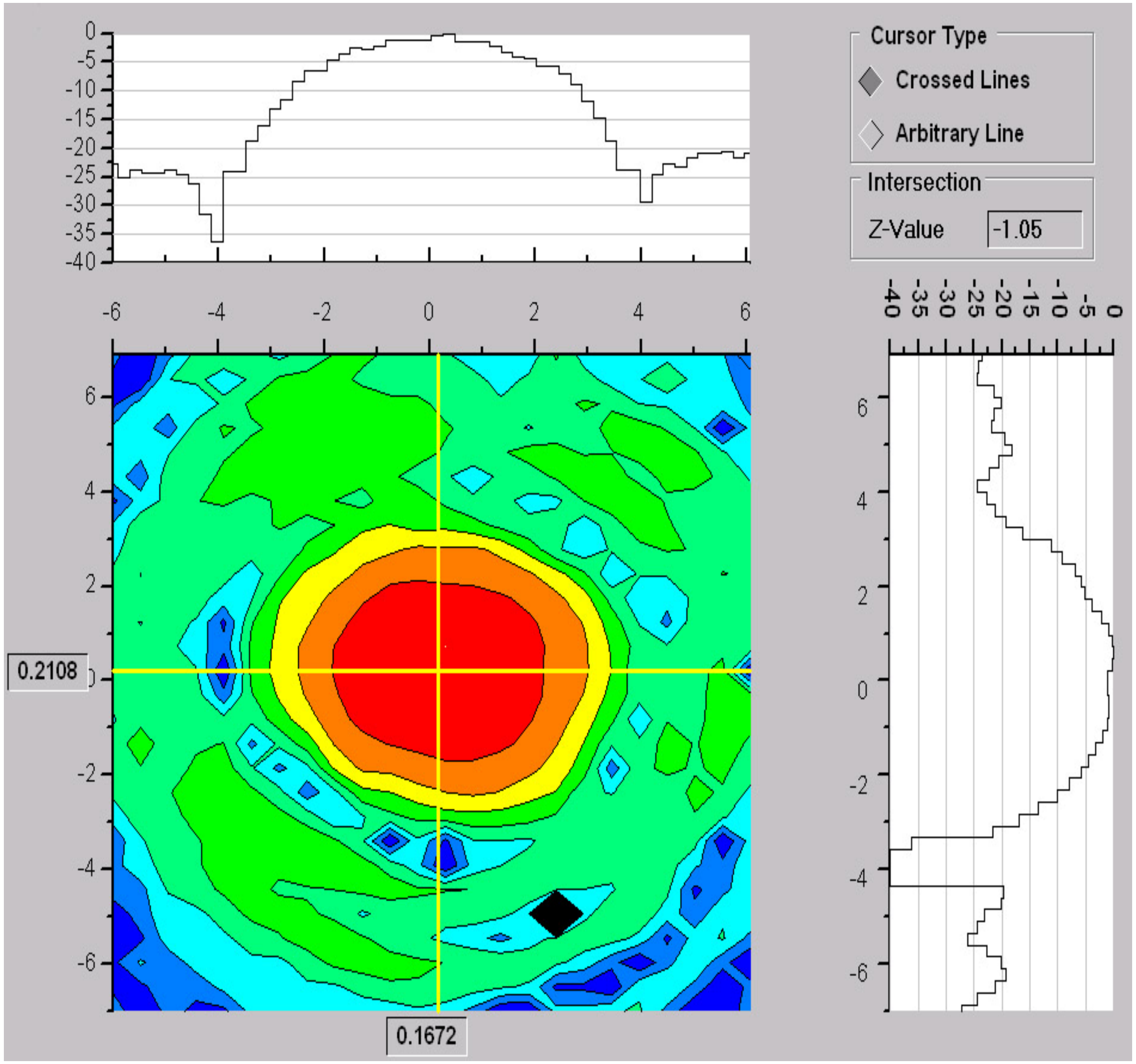
Tn (DSB) for different T3 designs (T bath =4.2 K;)



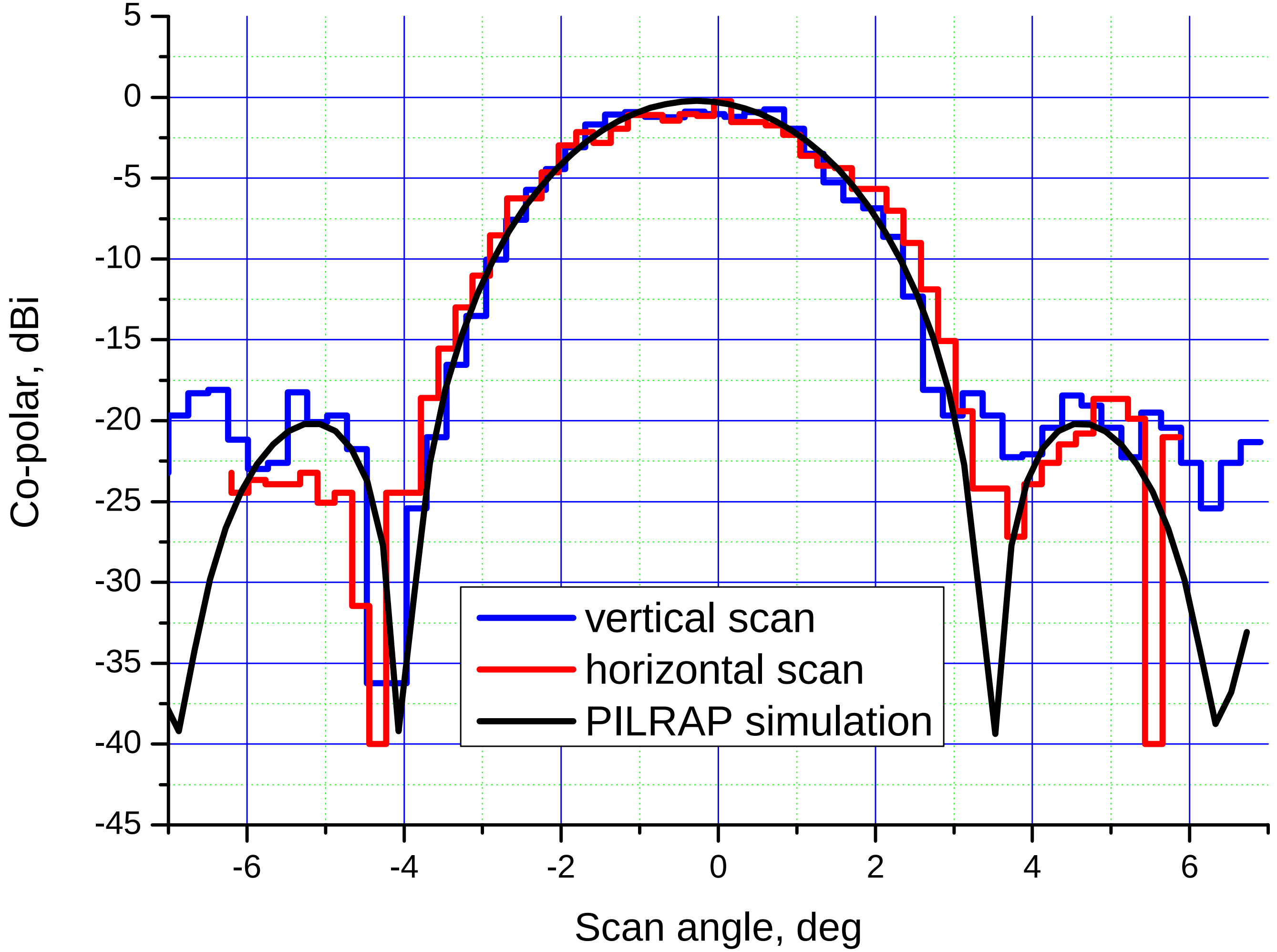
Noise Temperature (DSB), T3 - D2C1:
Red - T bath = 4.2 K; Blue – T bath = 2 K



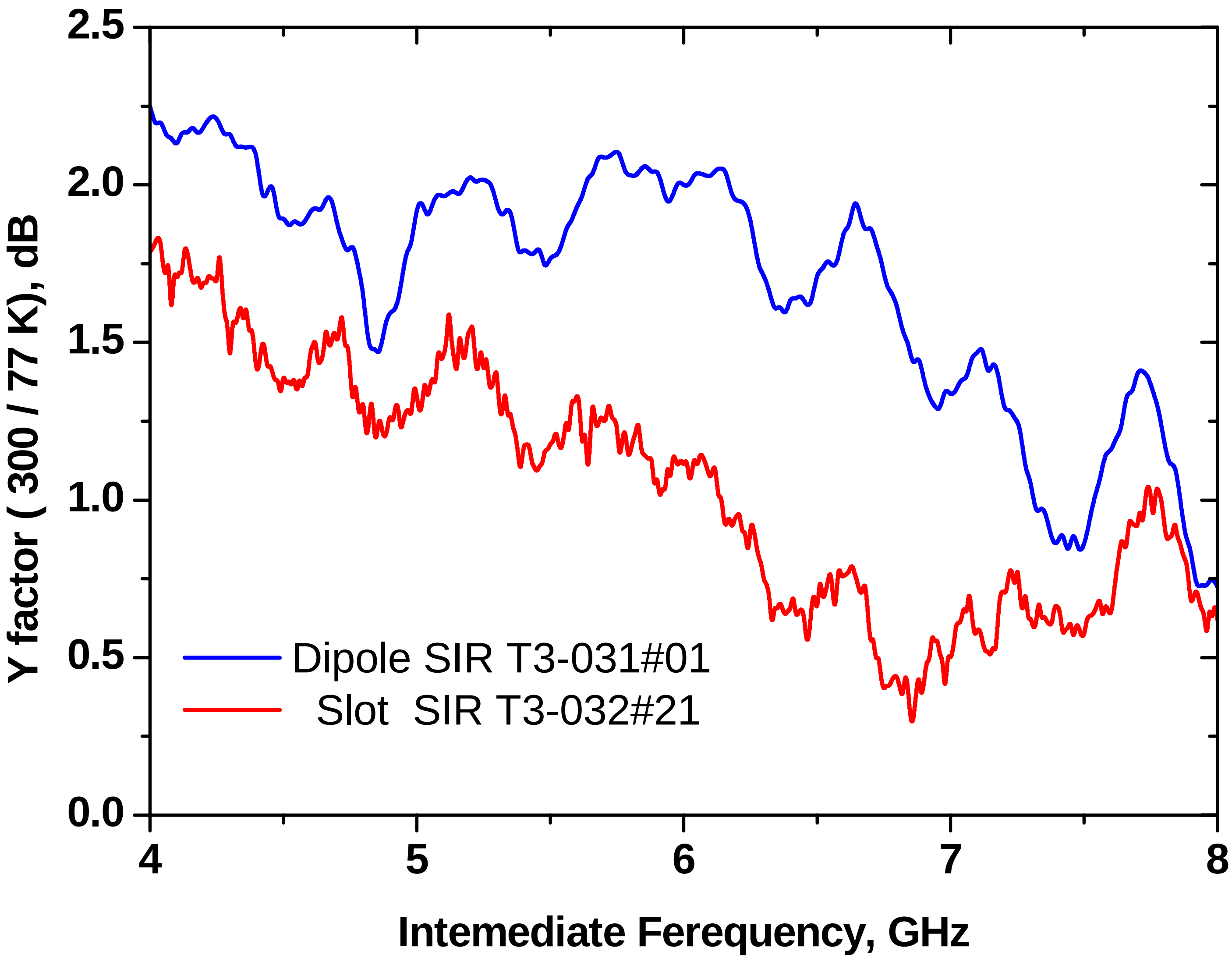
Beam Pattern of the SIR for TELIS



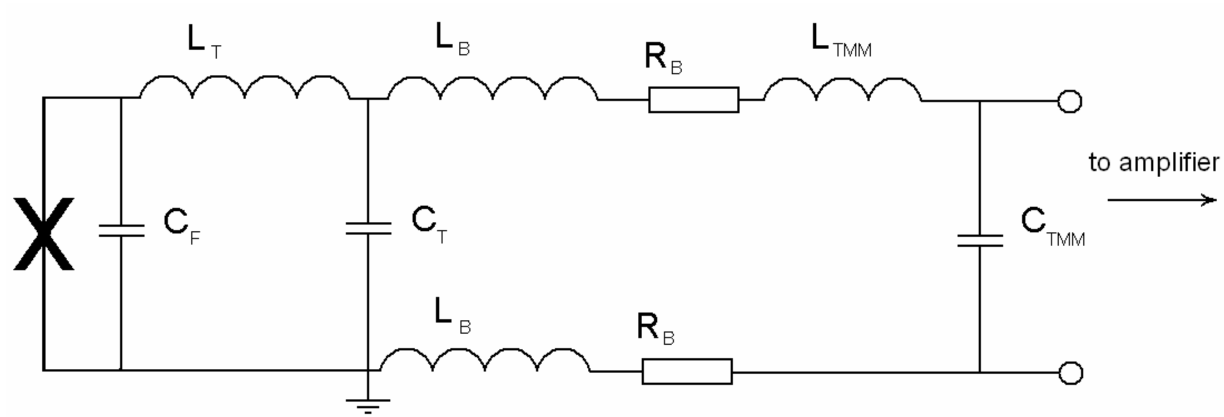
Antenna-lens beam pattern

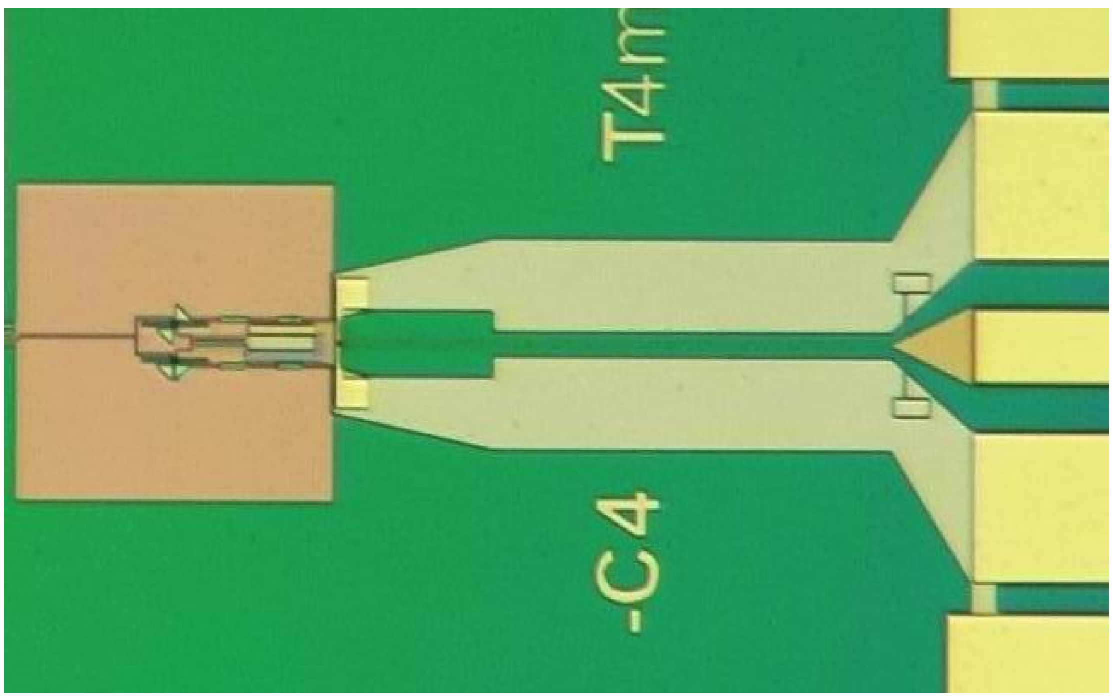


IF Performance of the T3 SIRs



SIR schematic diagram at IF





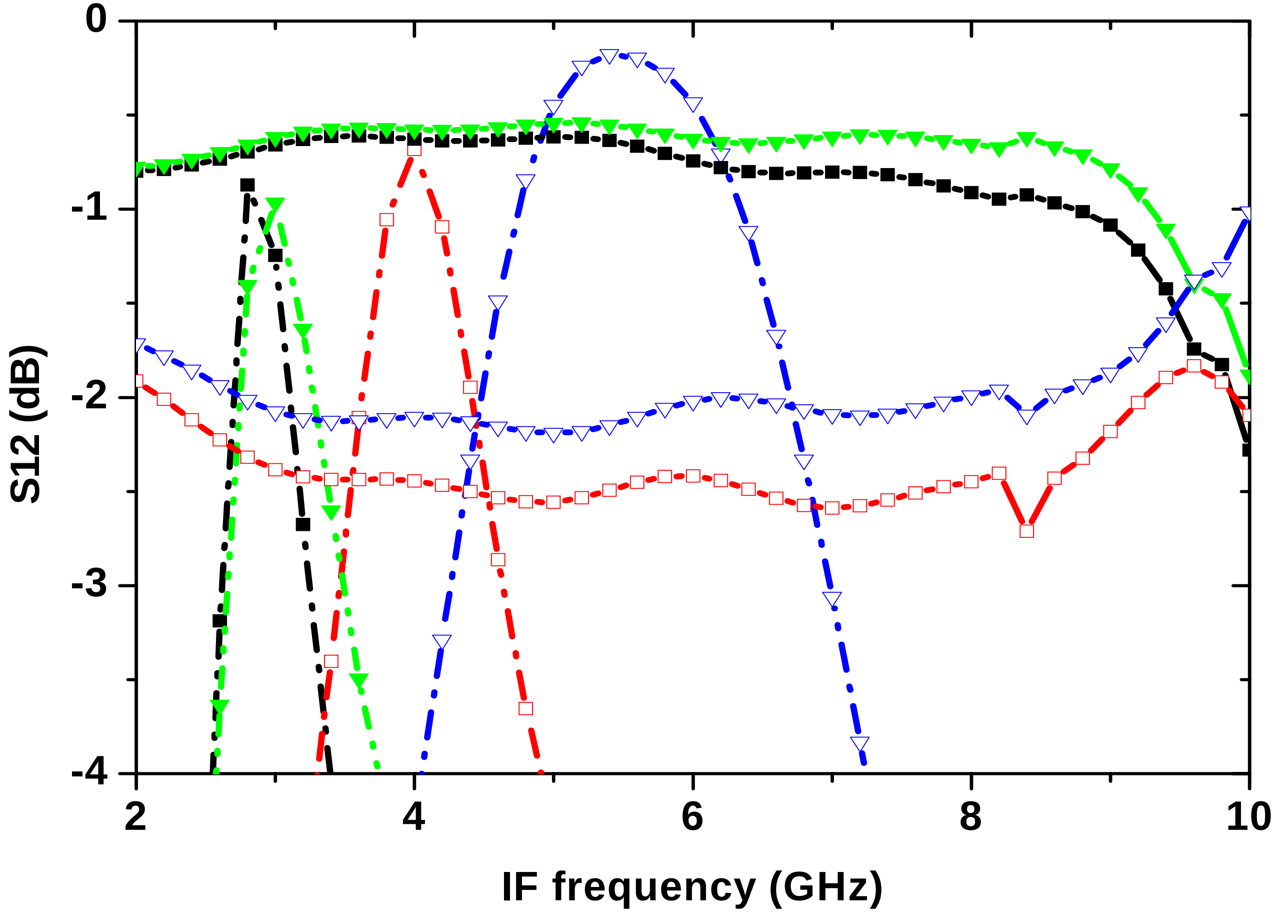
C_F – parasitic SIS-mixer and matching elements capacitance

L_T – tuning on-chip inductance (CPW line), **C_T** – tuning on-chip capacitor

L_B, R_B – bond wires inductance and resistance

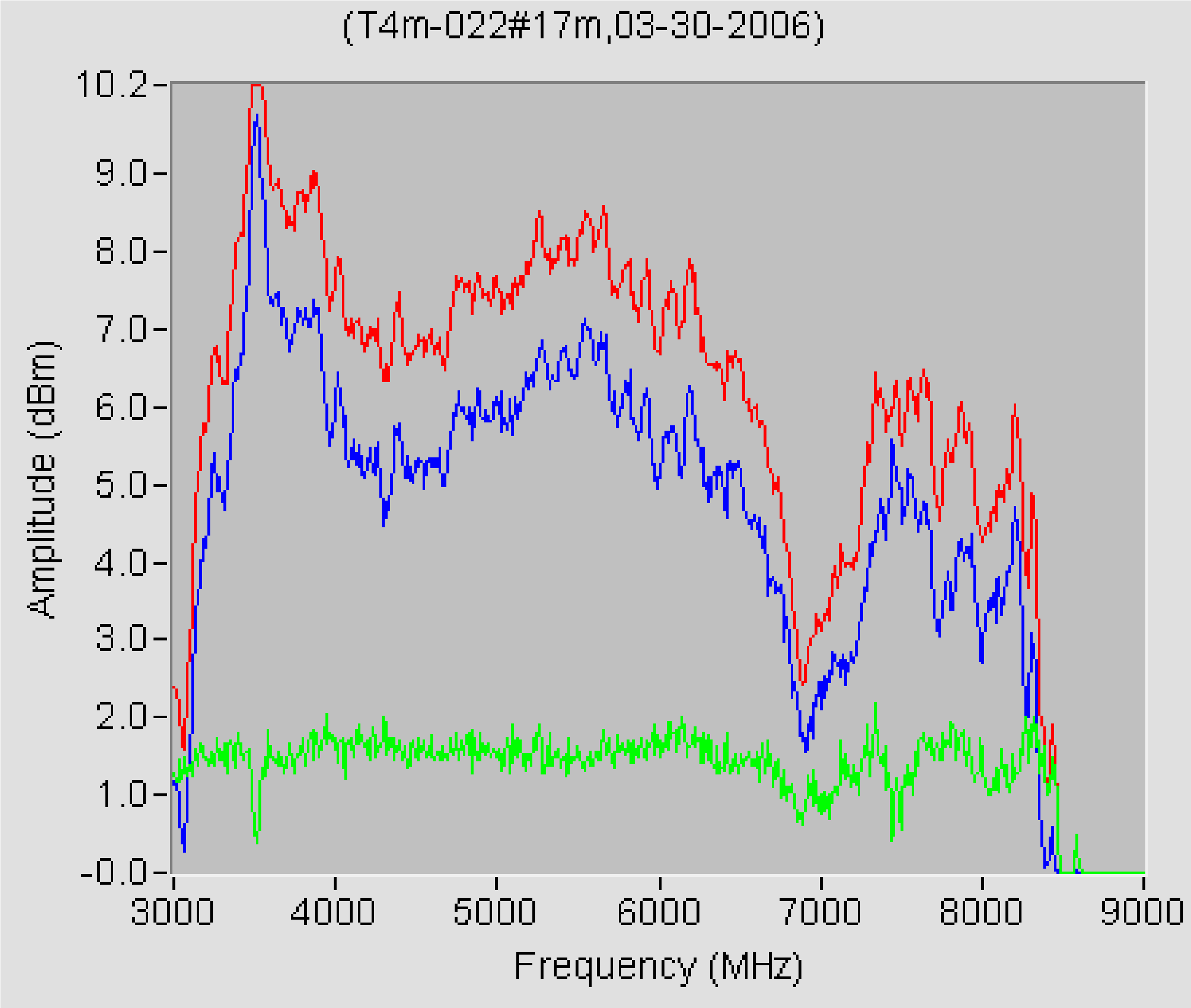
L_{TMM}, C_{TMM} – parameters for the microstrip line on the base (TMM) plate

Results of Sonnet simulations



Signal transmission by amplitude (S12 parameter) for the new wideband (soled lines) and the old narrowband (dash-dot lines) IF networks at the two values of SIS Rp

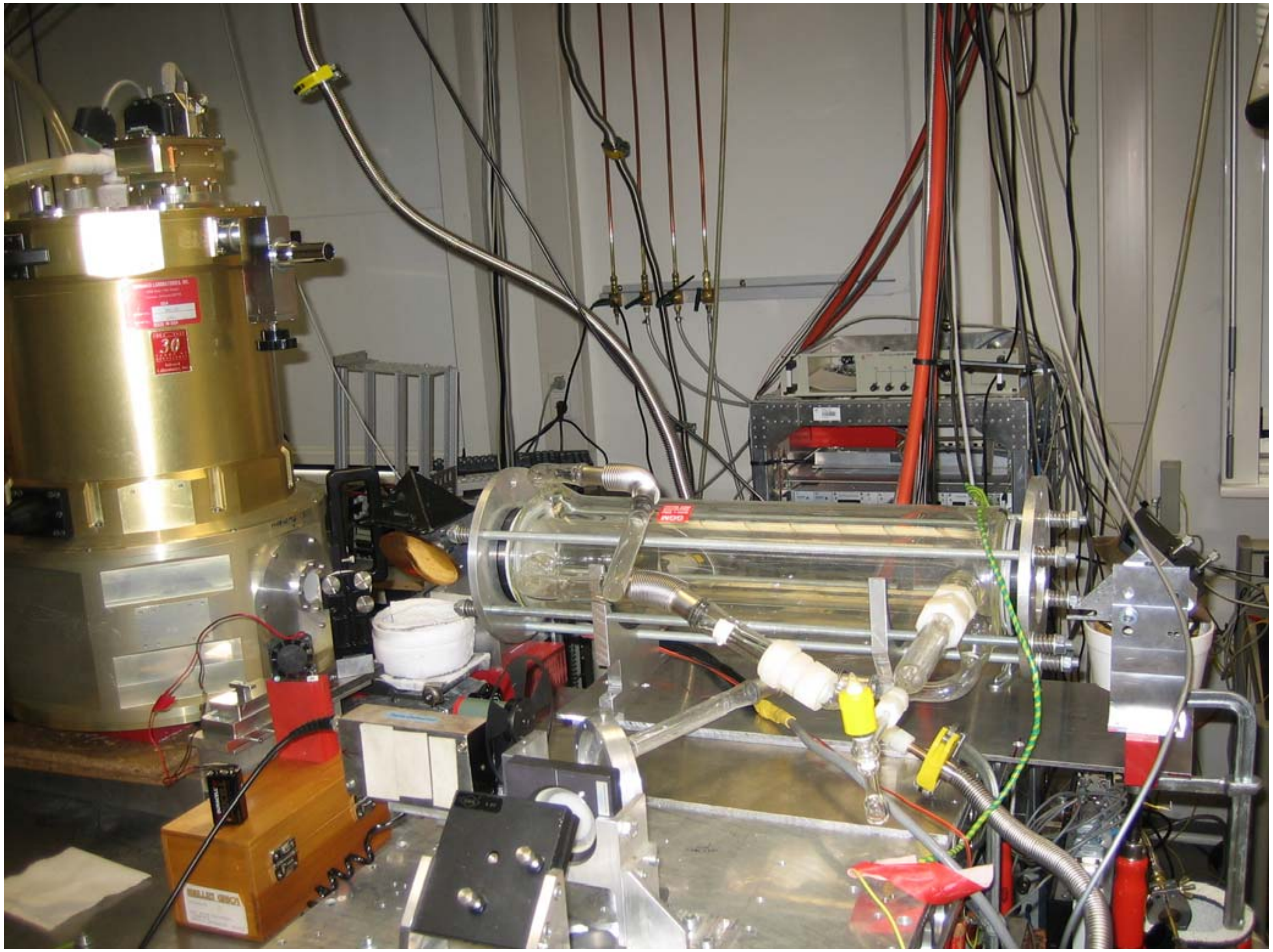
Experimental check of T4m IF performance



Noise measurements of the SIR with a slot-antenna.
SIS-mixer IF output at the hot (red curve) and the cold (blue curve) optical loads.
The green curve is the difference between them

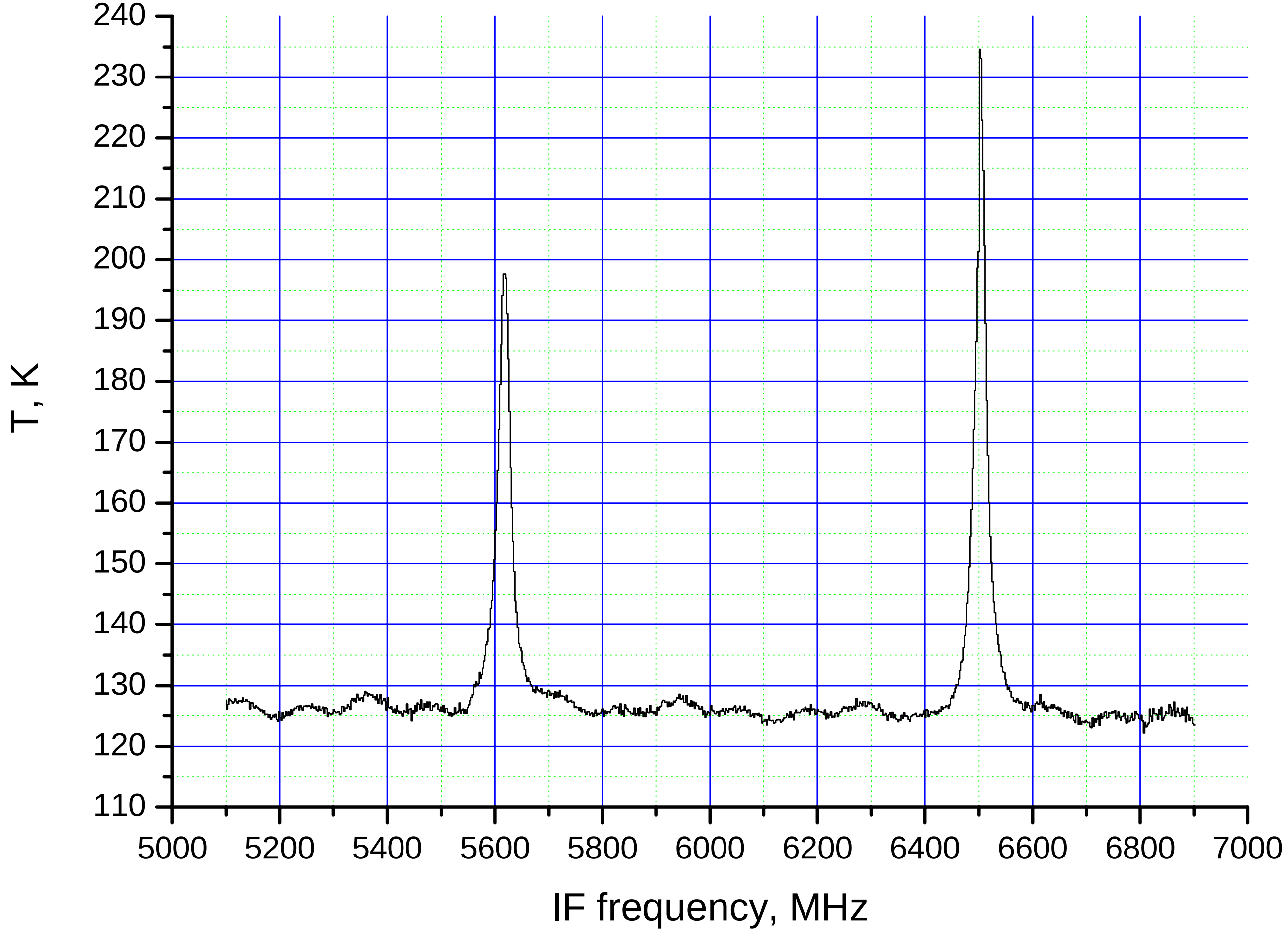
Noise breakdown: possible increase of the SIR Tn < 50 K

Photo of the gas-cell measurement setup at DLR

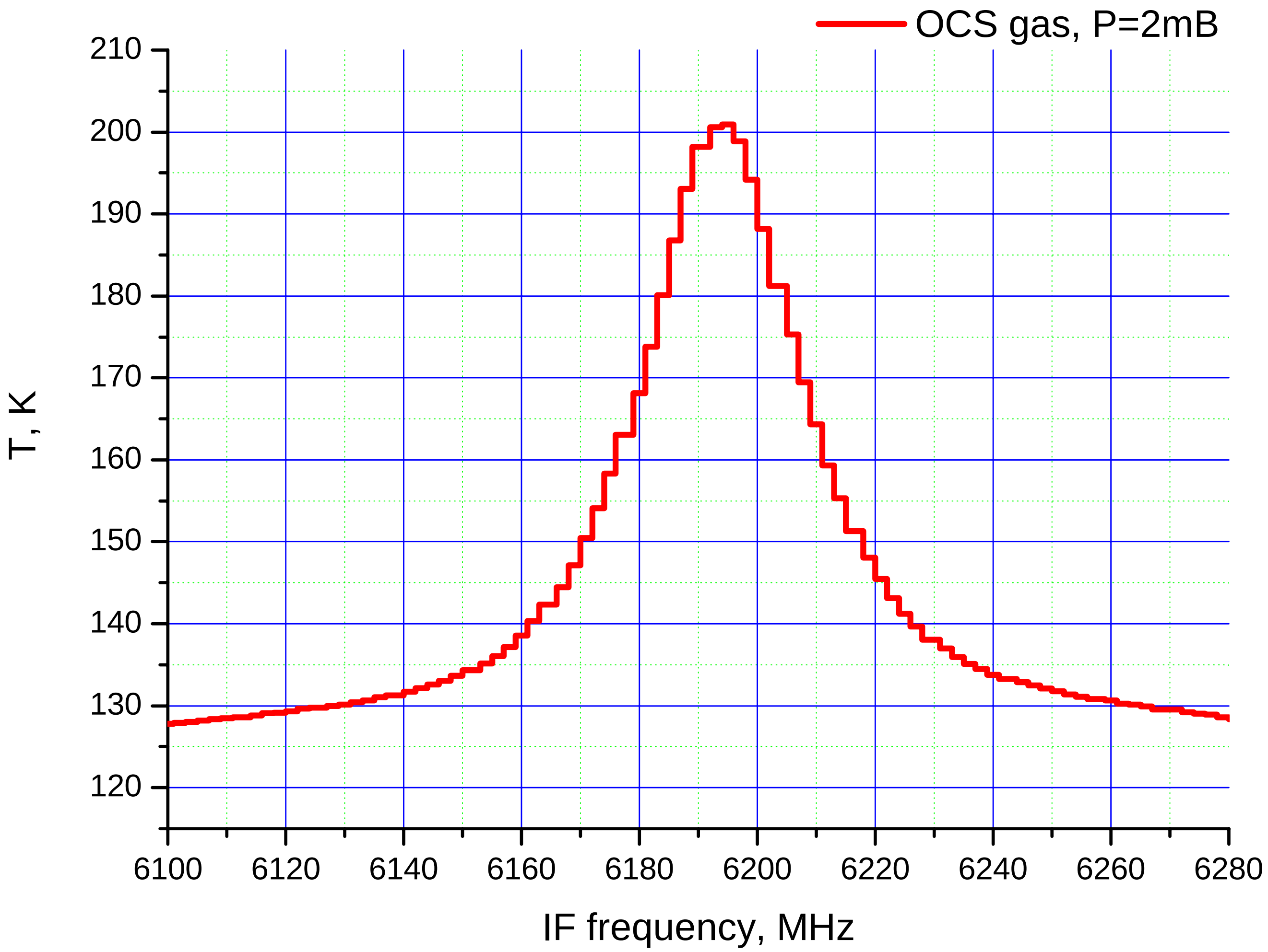


Deconvolved spectrum of two OCS emission lines

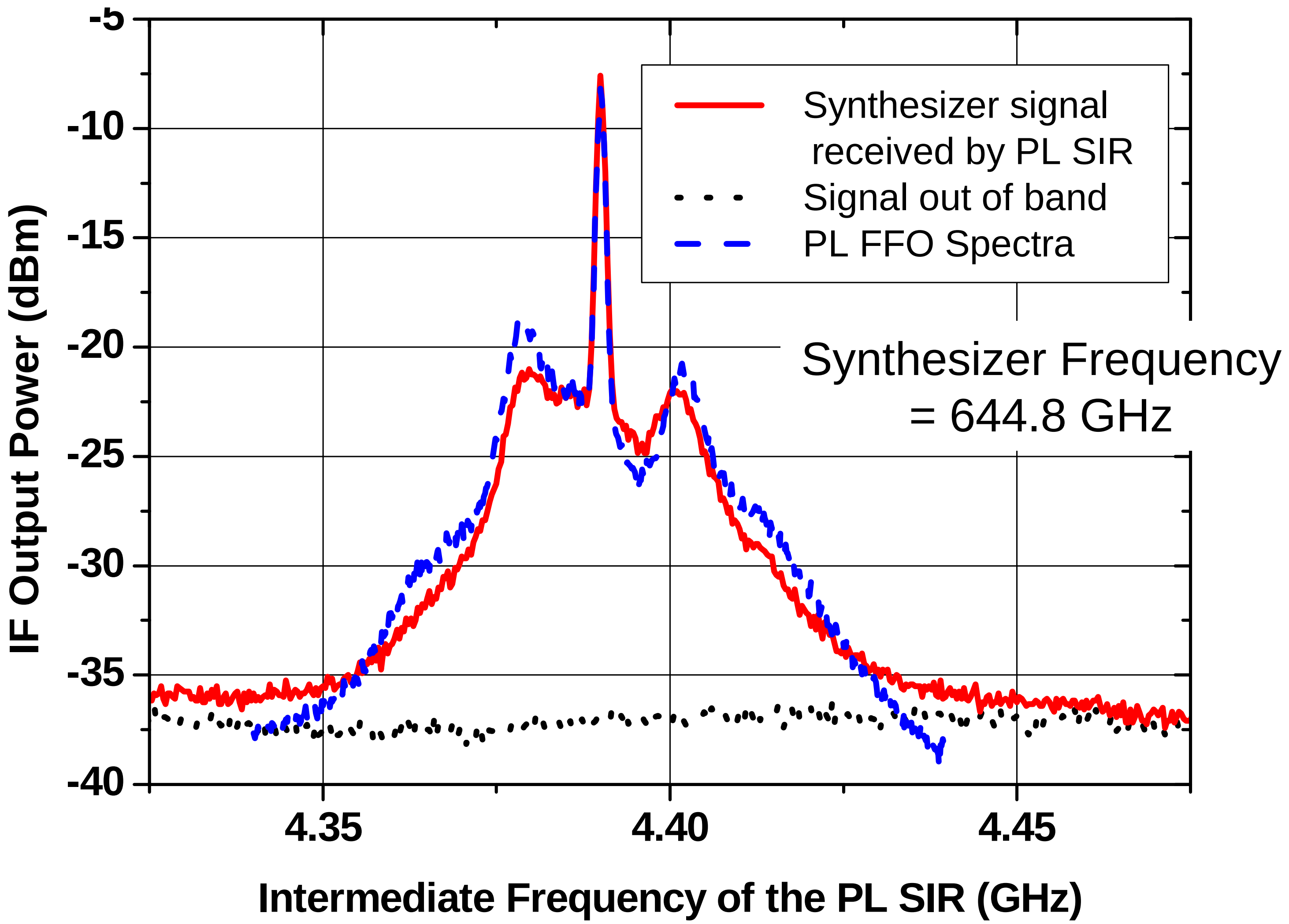
(gas pressure 1.2 mBar; FFO frequency 625.24 GHz)



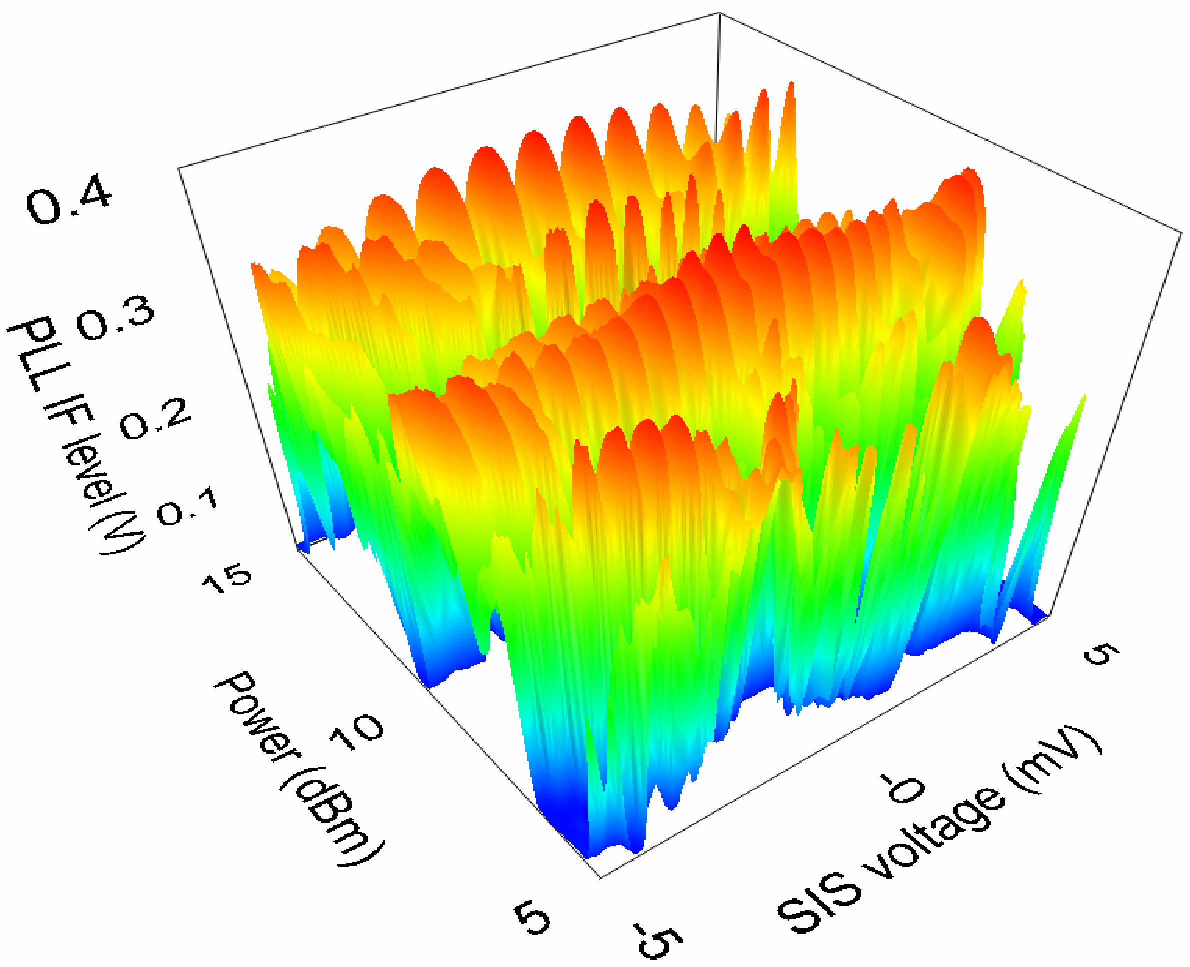
Gas cell measurements; resolution determined by DAC



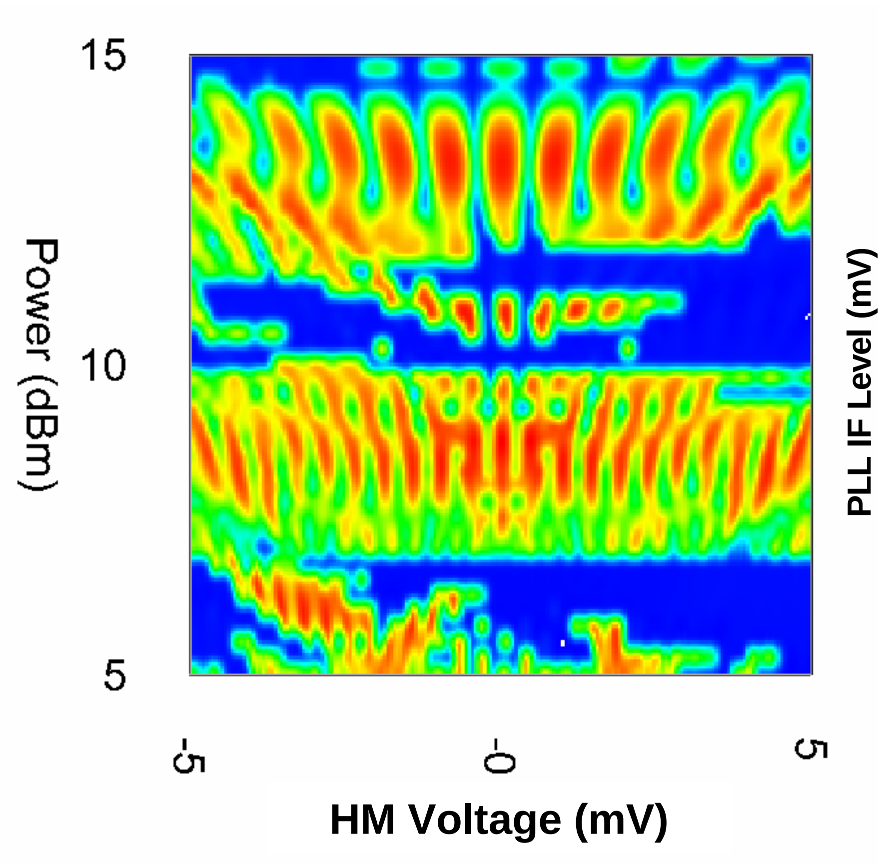
Phase locked FFO; spectral resolution < 1 MHz

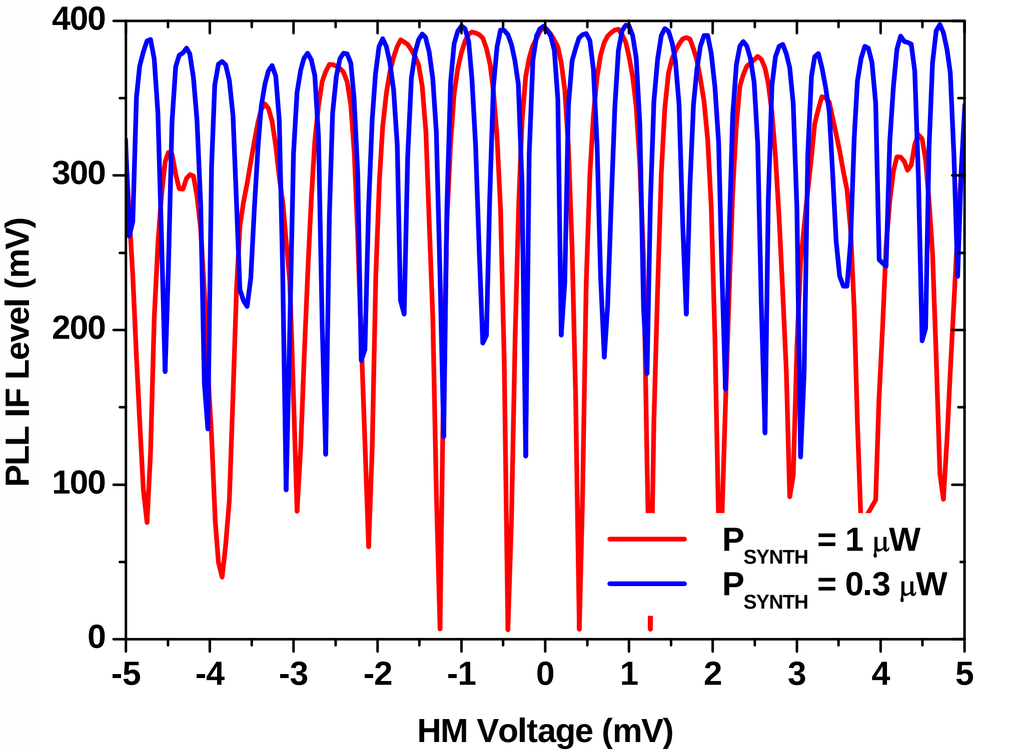


Remote optimization of the PLL SIR operation (3-D)

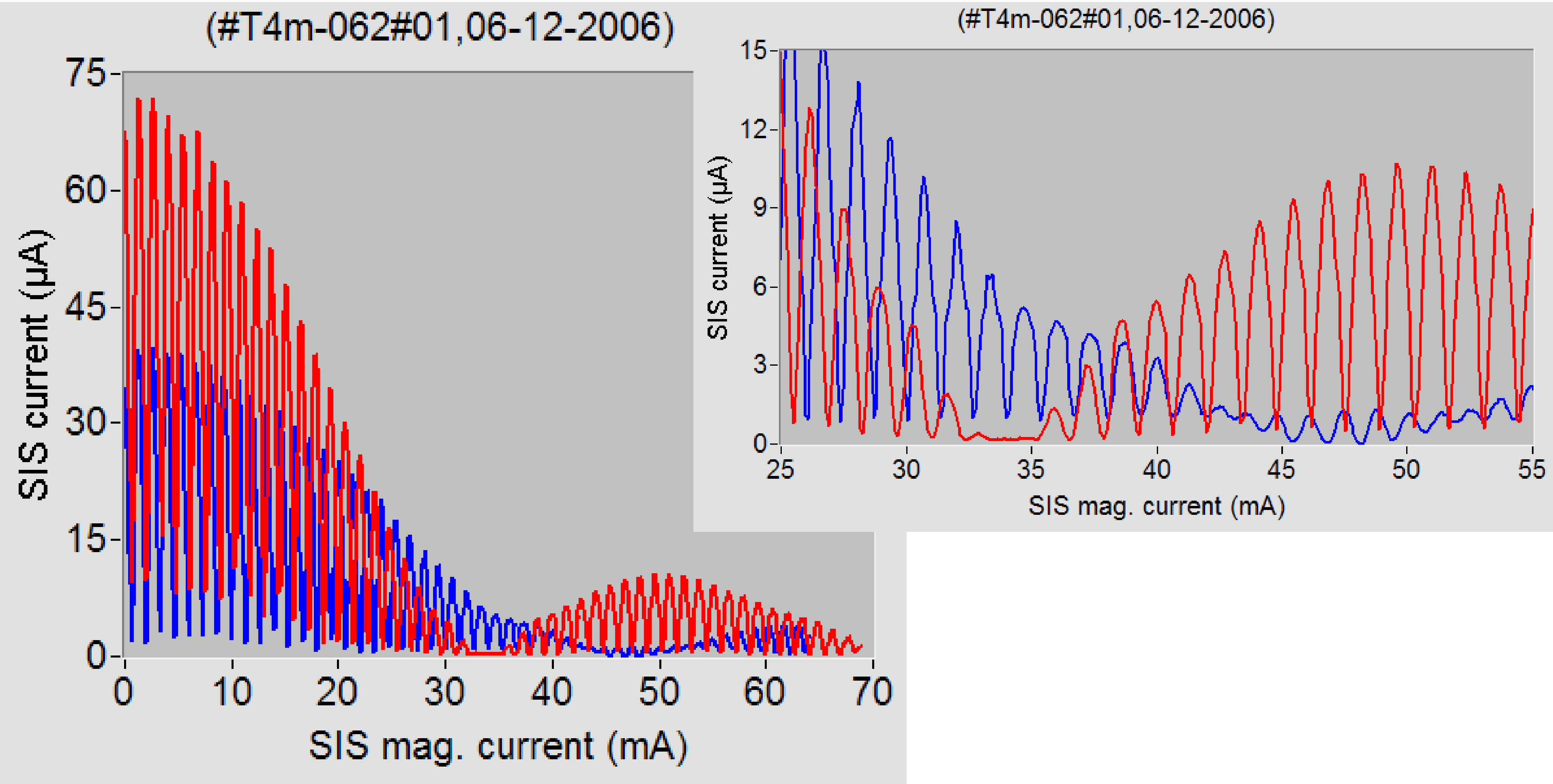


Remote optimization of the PLL SIR operation (2-D and 1-D)

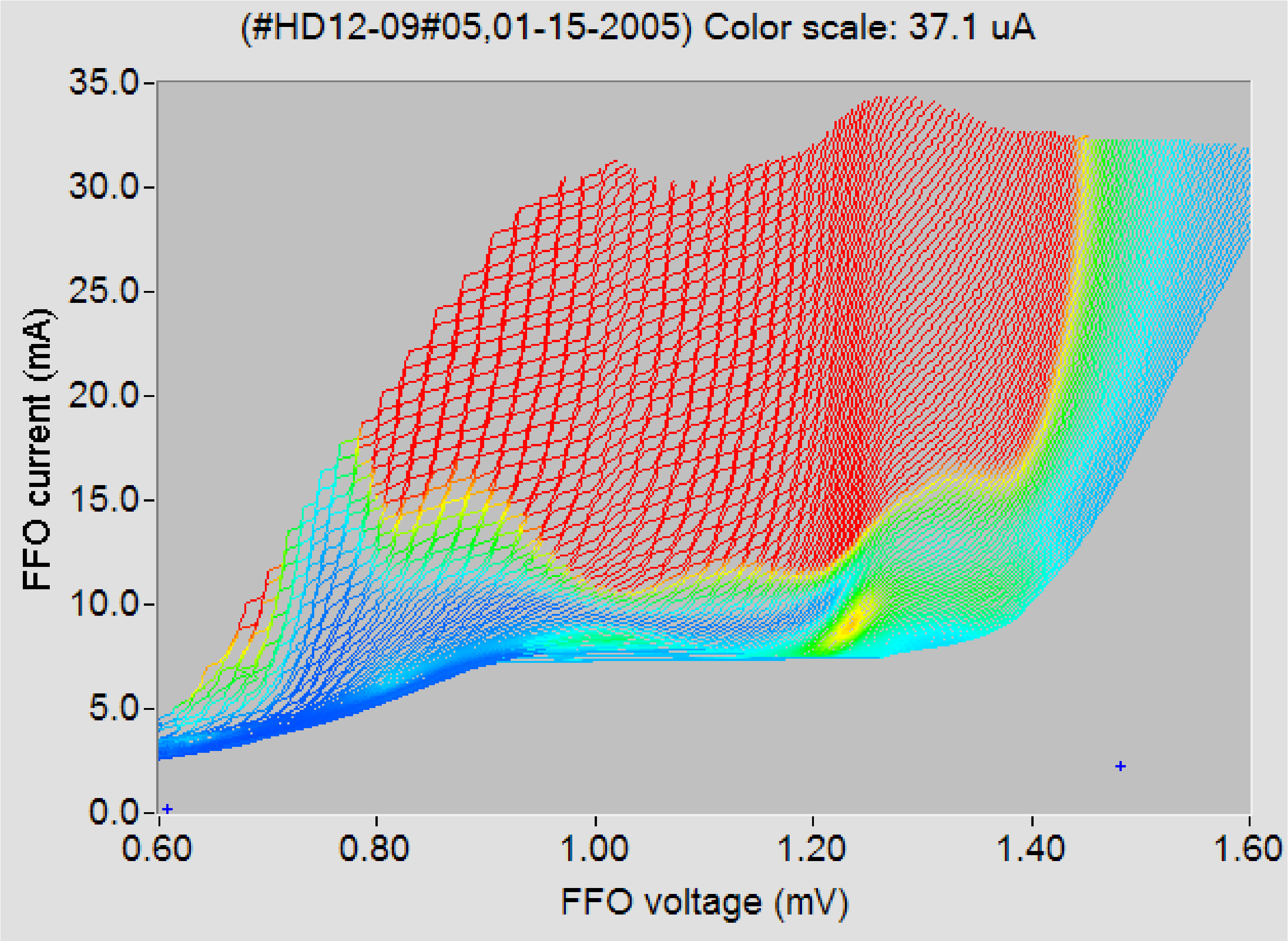




Ic (H) for twin SIS mixer - remote suppression of the SIS critical current by computer tuning

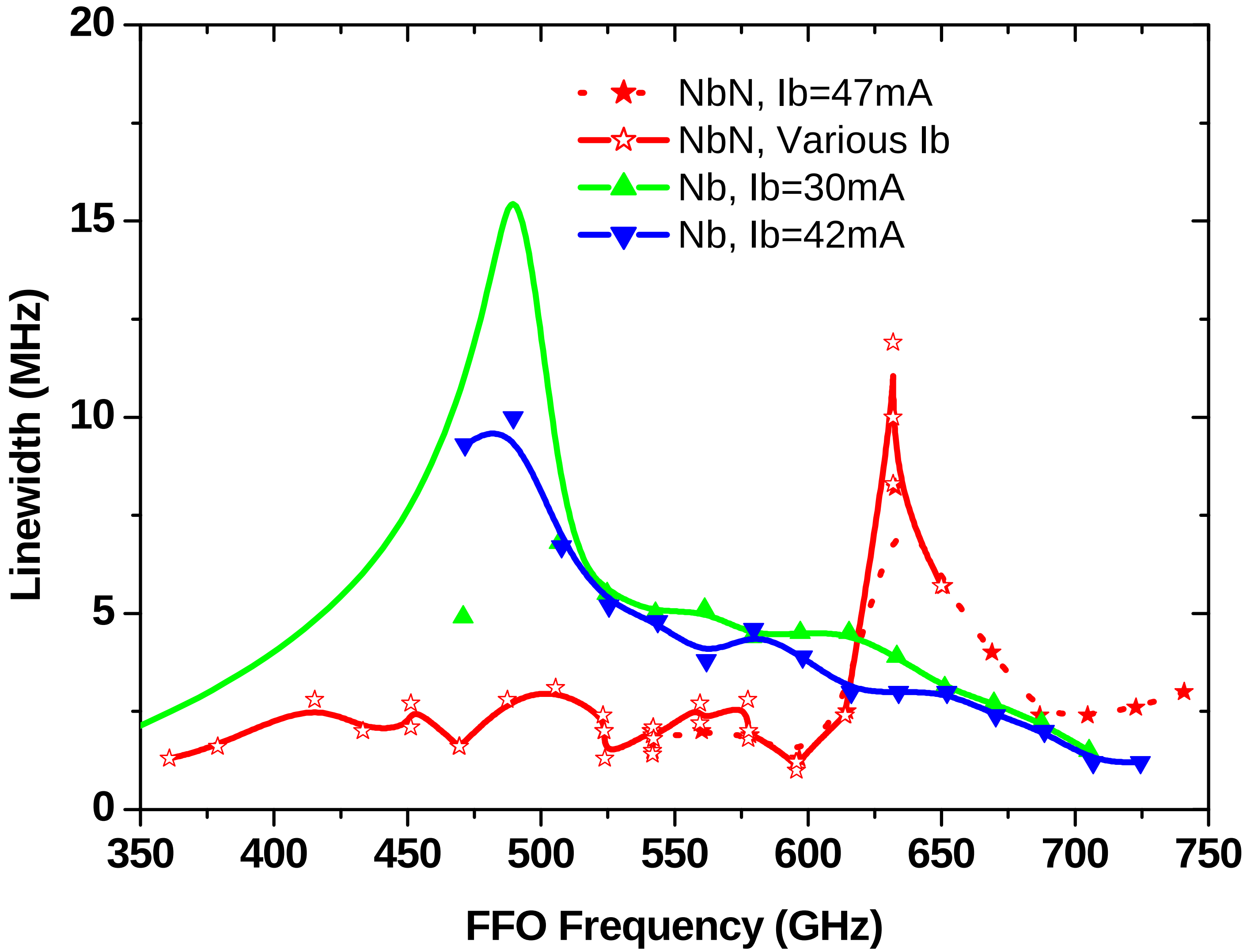


Nb-AlN-NbN SIR – new features



Wednesday, August 30, 2:00pm - 4:00pm; Report 3EG08

Nb-AlN-NbN circuits: LW on frequency



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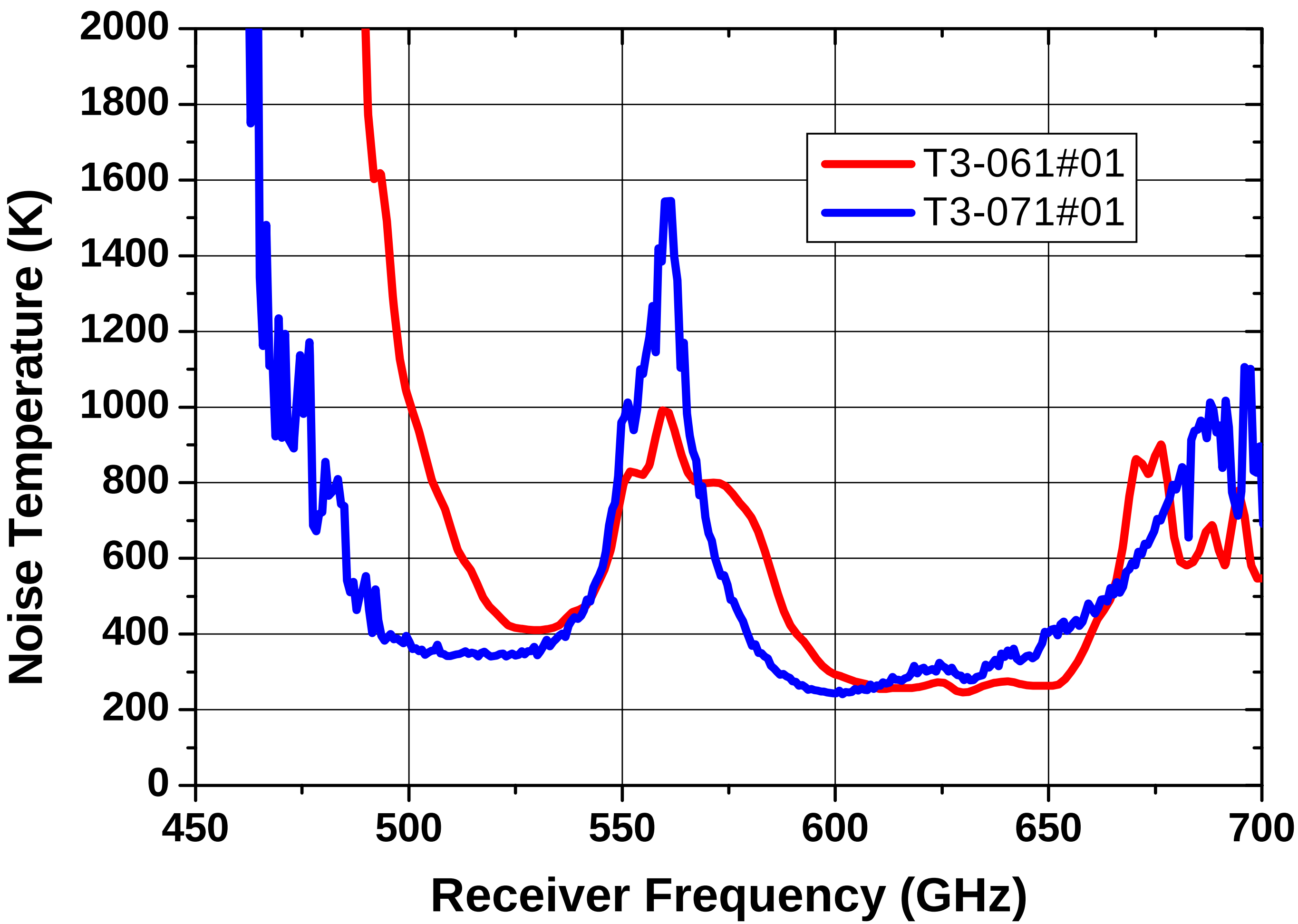
Nb-AlN-NbN SIR: Tn on FFO frequency



Wednesday, August 30, 2:00pm - 4:00pm; Report 3EG08

SIR for TELIS - Conclusion

- **TELIS requirements can be realized for already developed designs and existing technology:**
- **Uncorrected receiver DSB noise temperature is of about 250 K at 600 GHz for SIR with phase-locked FFO;**
- **IF bandwidth 4 - 8 GHz was proven, Tn increase < 50 K**
- **Beam pattern: FWHM = 3 deg, Sidelobes – 17 dB**
- **Improved design of the FFO for TELIS:**
  free-running linewidth from 9 to 2 MHz (500 – 710 GHz)
  that allows to phase lock from 35 up to 90 % of FFO power.
- **Spectral resolution < 1 MHz (< 3 MHz in flight due to DAC)**
- **Procedure for remote optimization of the PL SIR operation has been developed and experimentally proven**
- **New Nb-AlN-NbN SIRs (ready for first TELIS flight):**
  Frequency range 350- 700 GHz; Tn < 250 K;
  LW < 3 MHz (350-600 GHz), below 10 MHz (600-700 GHz)
- **First qualification TELIS flight is foreseen in 2007**