SIR for TELIS (post-critical review)

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List of participants

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SIR for TELIS (post-critical review)

- **Four Technical Notes, distributed after April 2004**

1. **FFO power and linewidth (dependence on design and FFO parameters)**
2. **Optimization of the HM and PLL operation**
3. **Results of preliminary tests of T2 SIRs and mixer cryostat electronics (including TMM)**
4. **Numerical simulation of an SIS mixer output spectrum. Dependency of an SIR resolution and dynamic range on autonomous FFO LW**

- **Considerable improvement of the IREE technology**

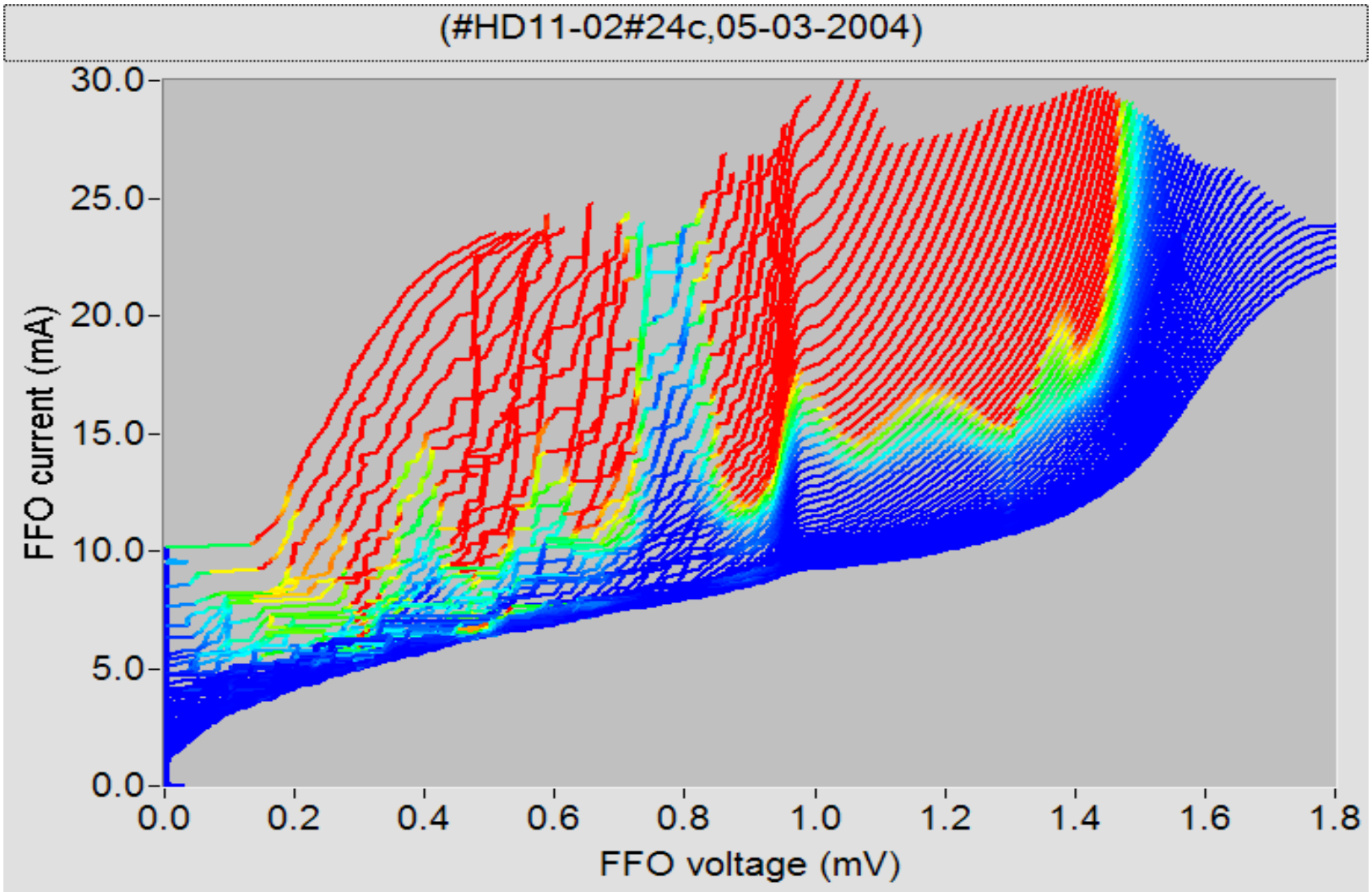
  (SIR yield for batch T2m-031 > 90 %)

- **First T2m devices were tested as a receiver with PL**

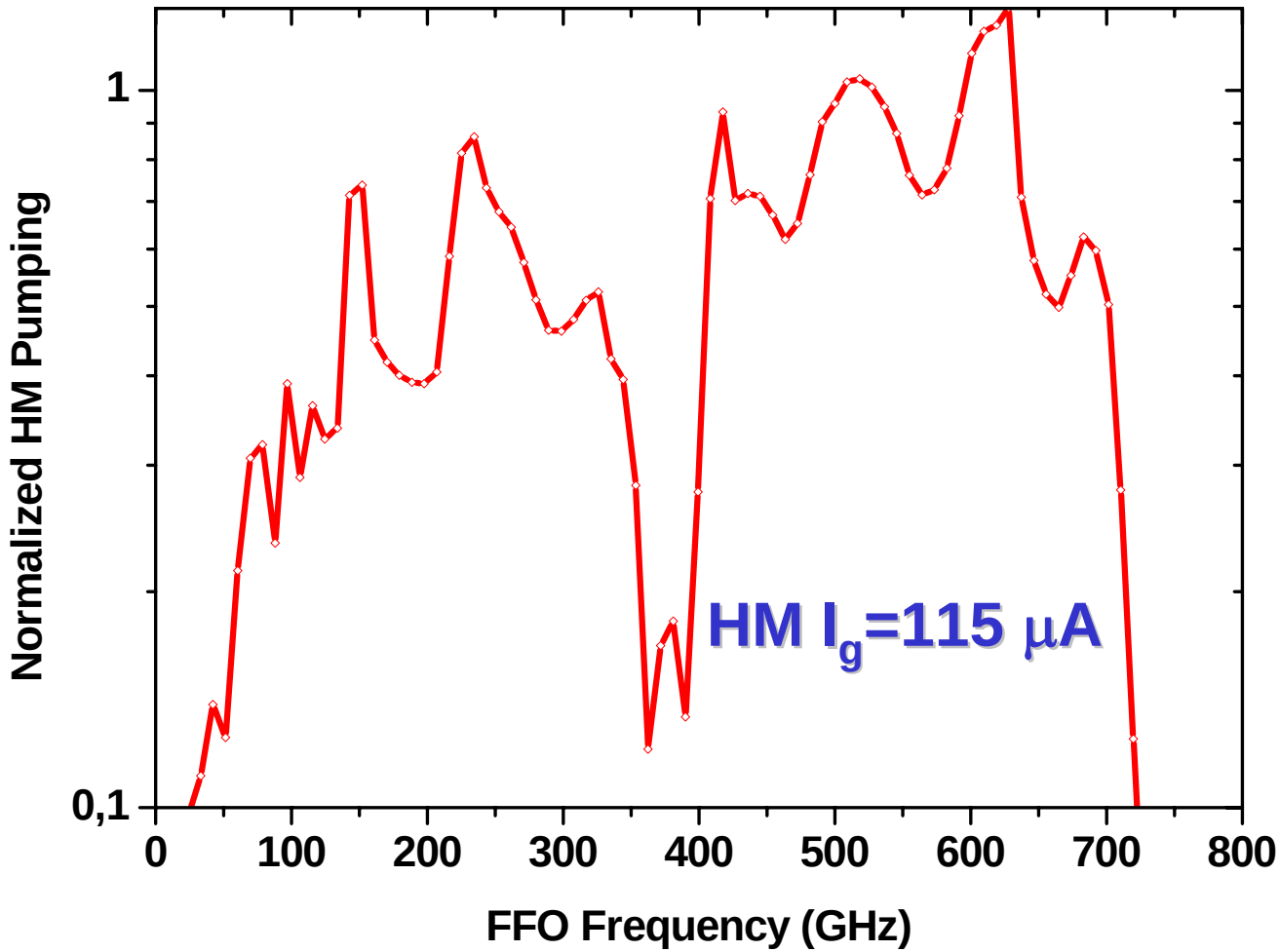
  Uncorrected receiver DSB noise temperature is of about

  500 K at 600 GHz and 630 K at 680 GHz

IVCs of the FFO of HD 11 design, measured at different magnetic fields

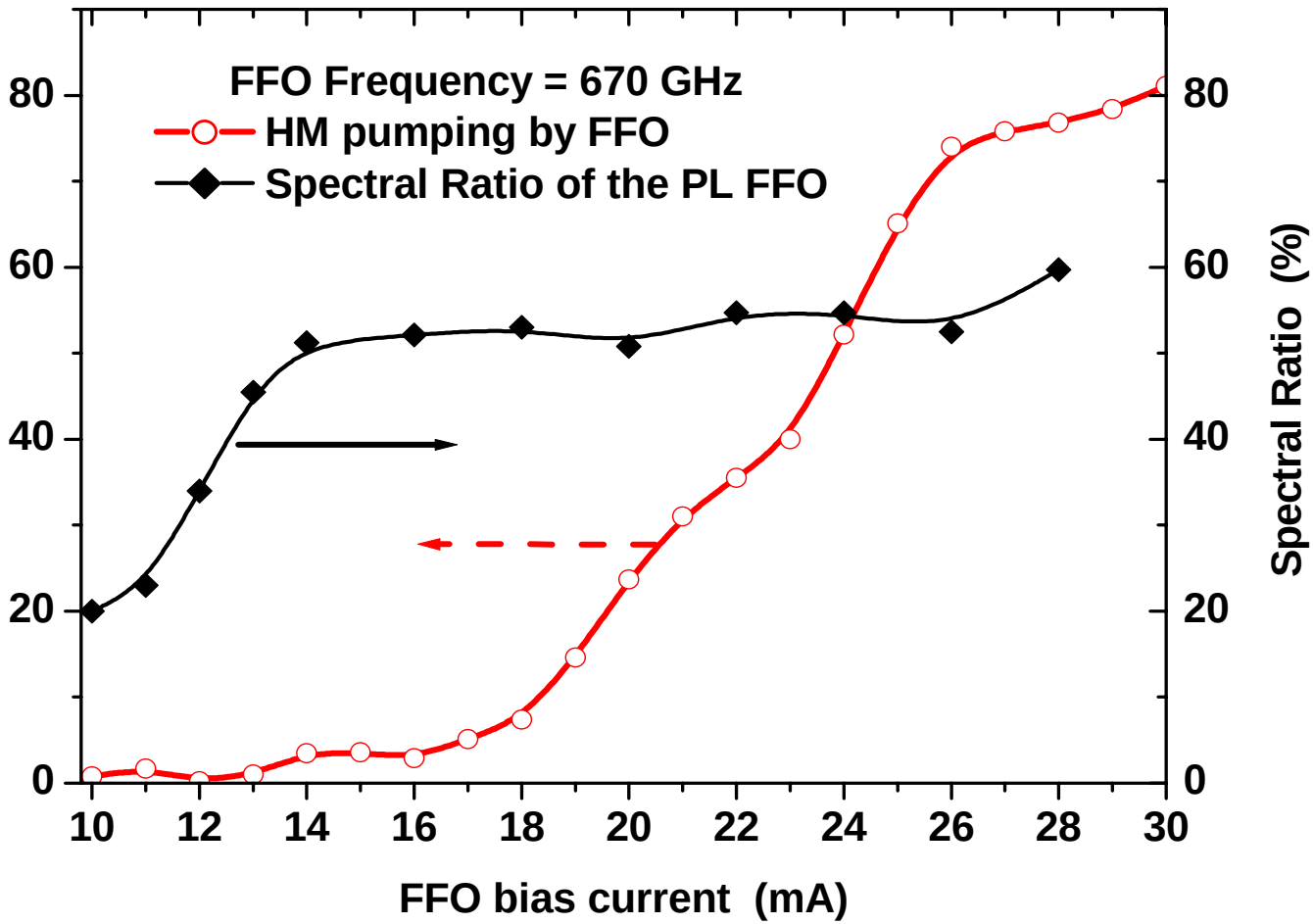


Dependence of the HM current (HM pumping) induced by FFO (HD-11) on the FFO frequency

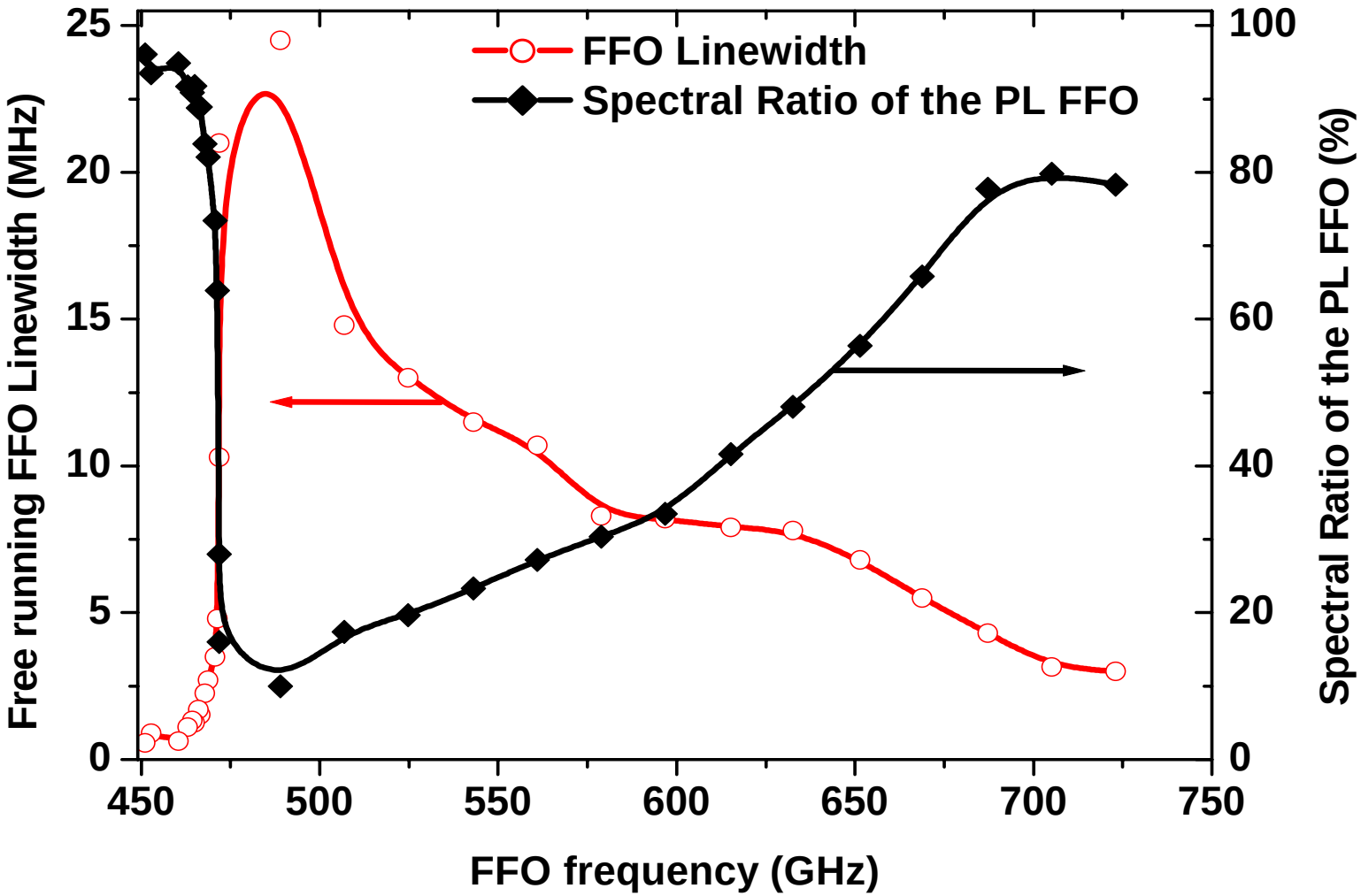


HM pumping and Spectral Ratio of the PL FFO as a function of FFO bias current.

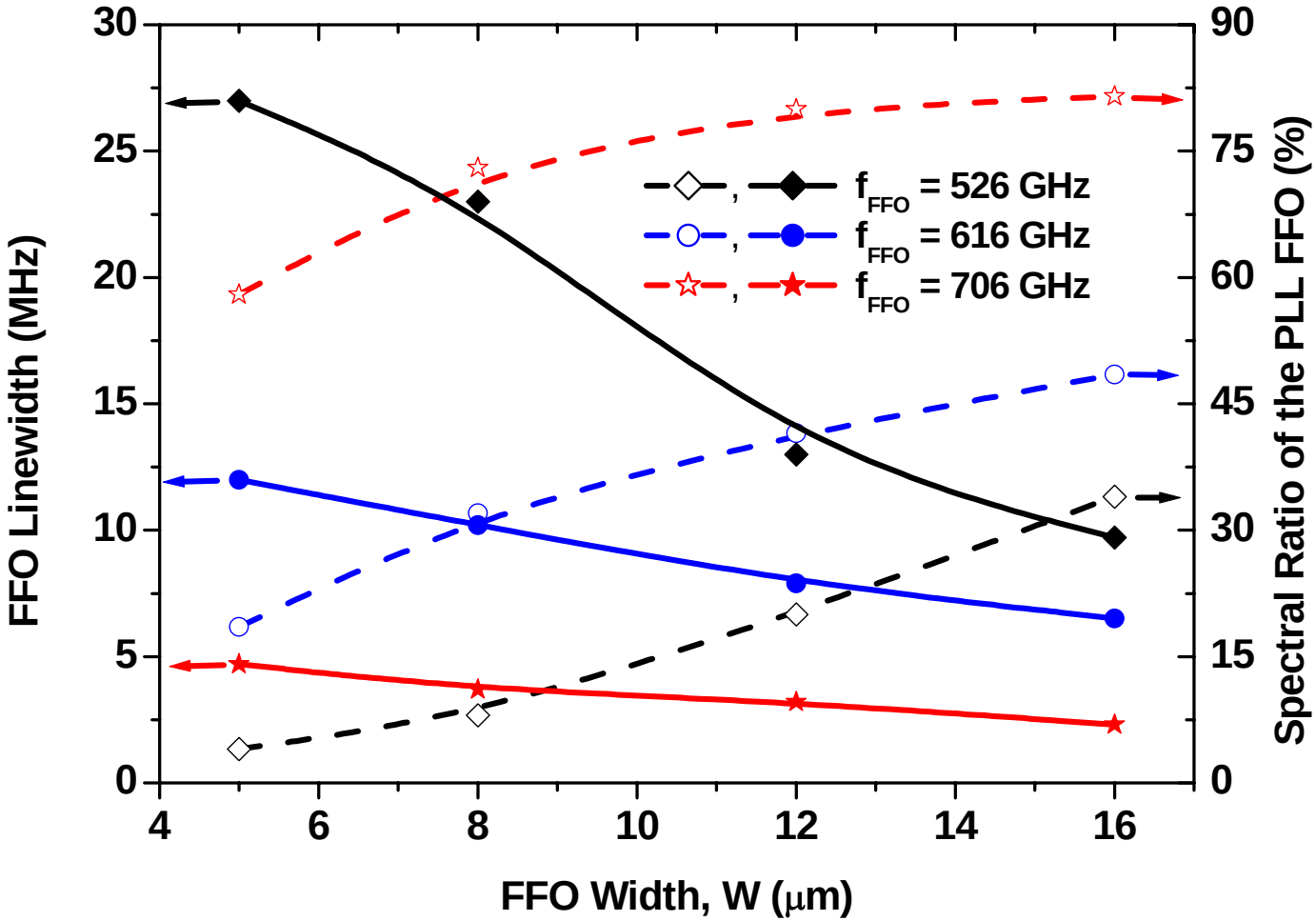
FFO frequency 670 GHz



FFO linewidth and Spectral Ratio PL FFO on its oscillation frequency.

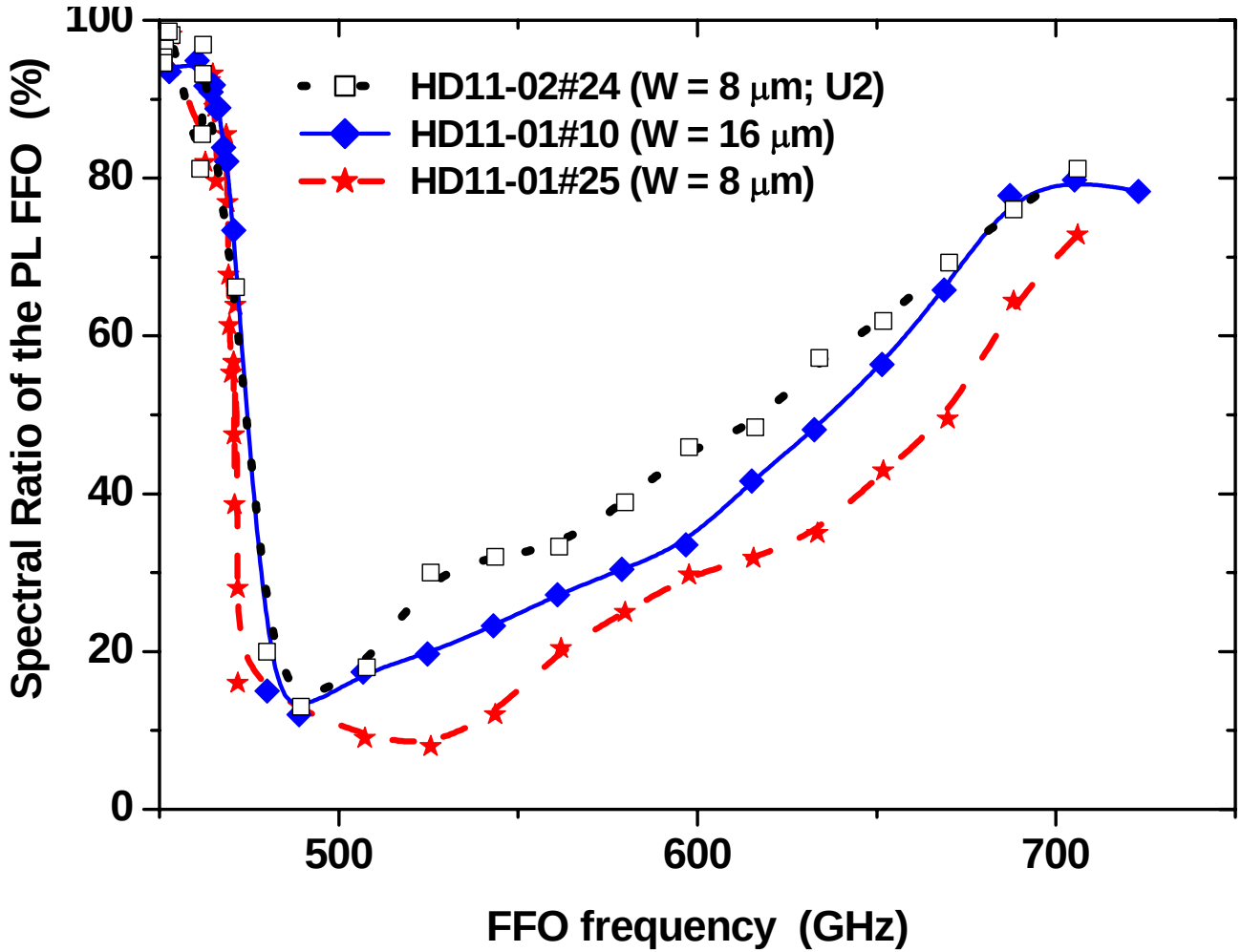


Linewidth of free-running FFOs and SR for the PL FFO as a function of FFO width.

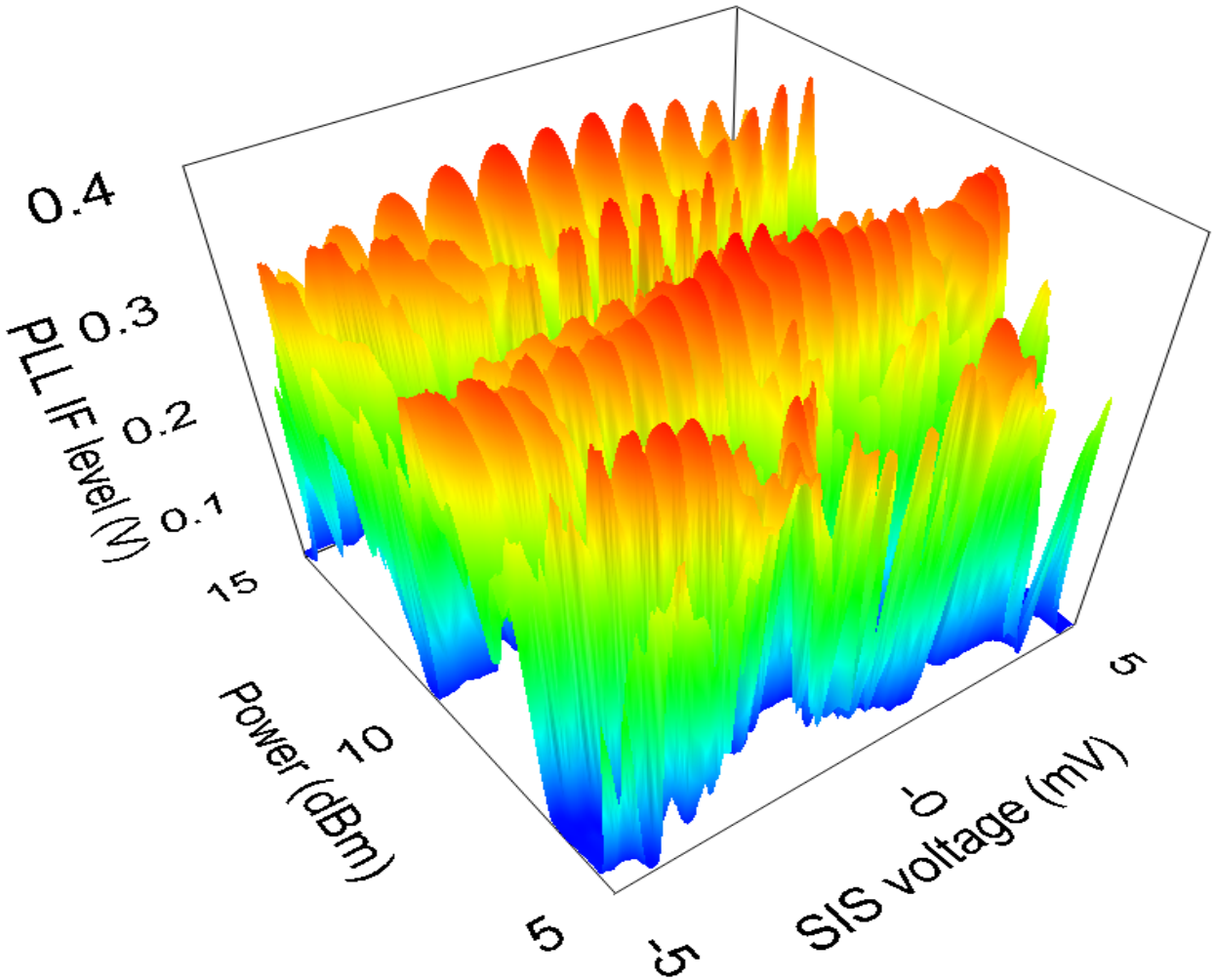


SR of the PL FFO with increased overlapping

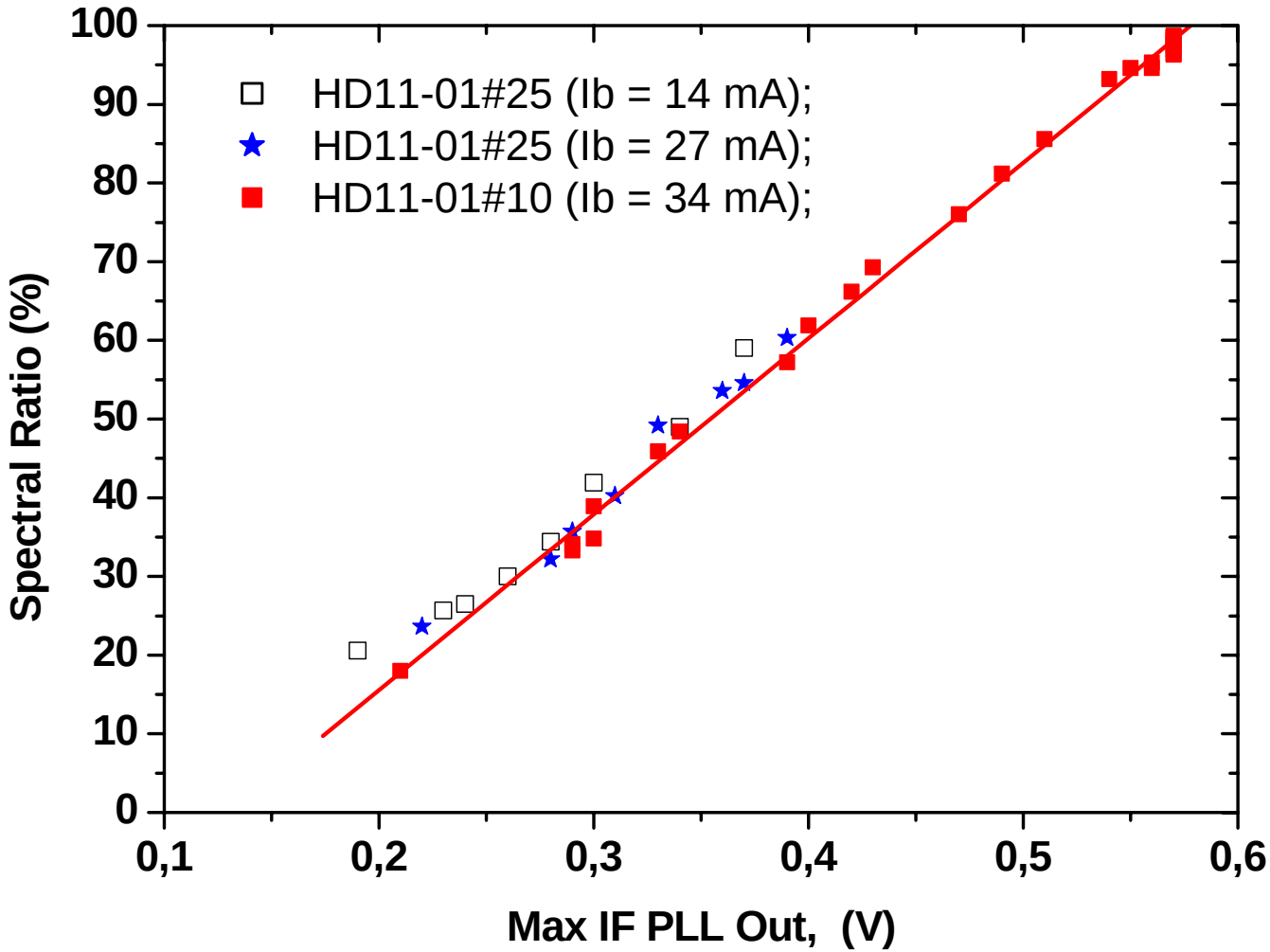
All circuits are from the same batch, Jc= 7 kA/cm^2



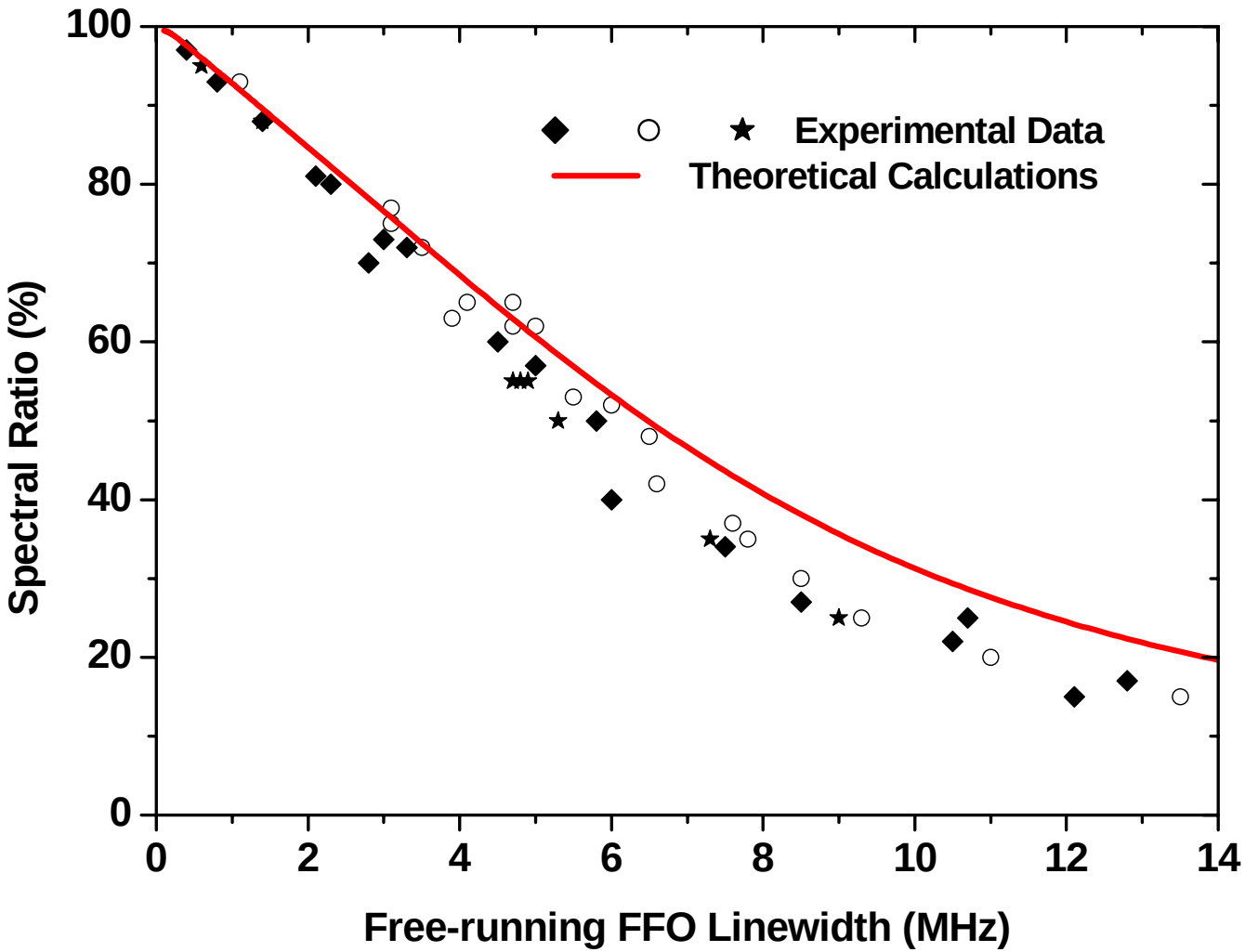
Remote optimization of the PLL SIR operation (3-D)



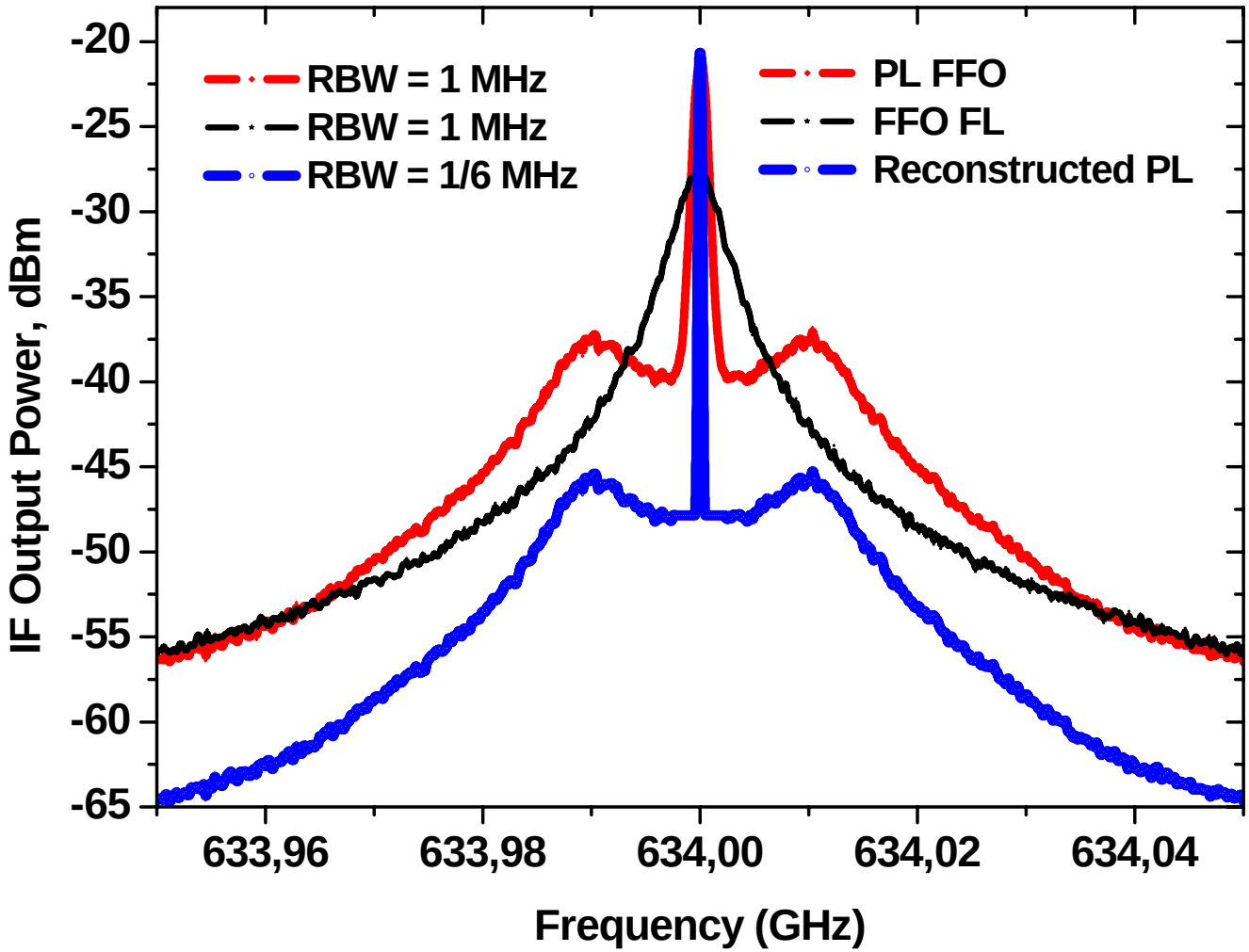
Spectral ratio of the PL FFO vs IF level output of the PLL system



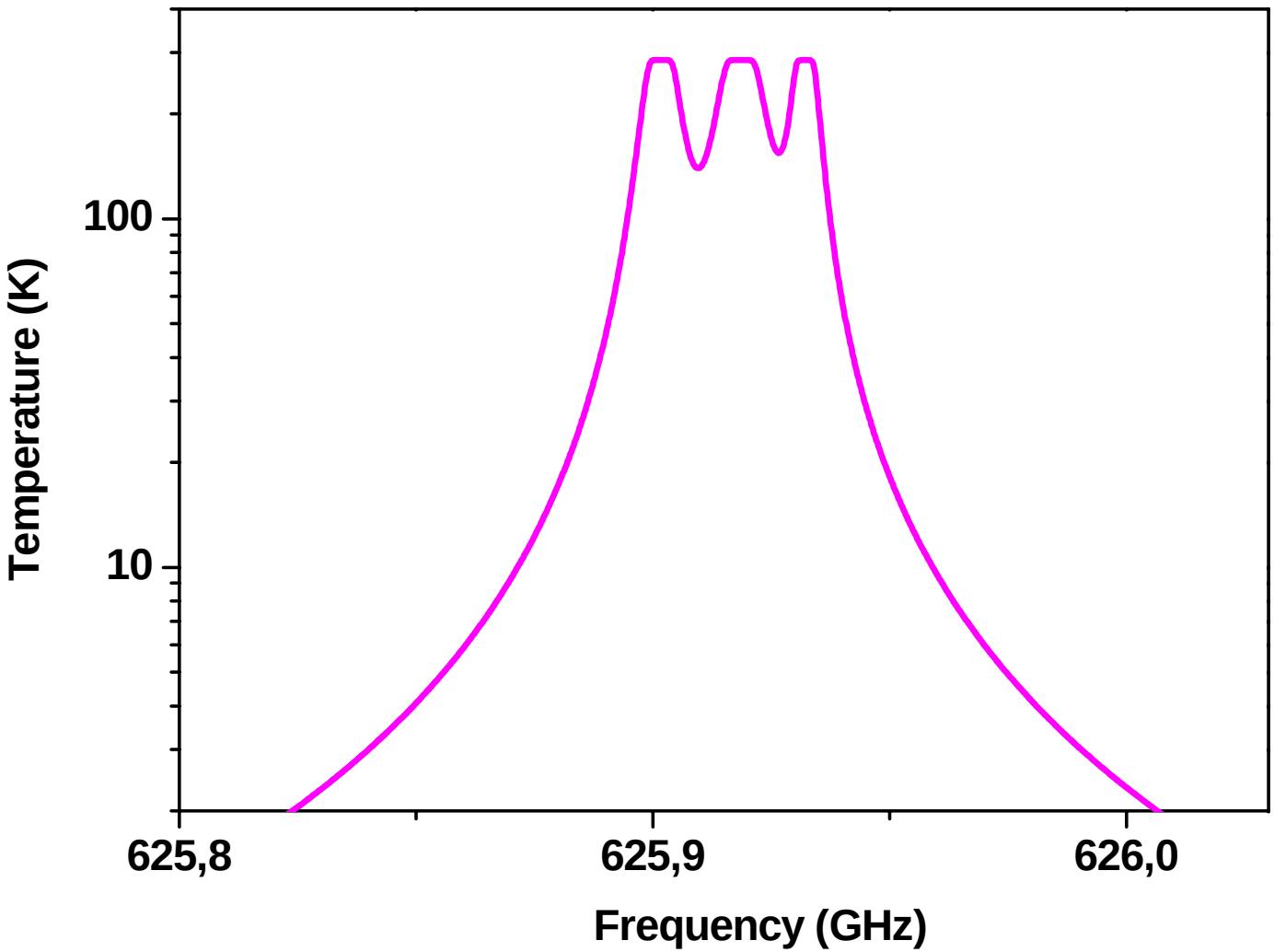
Spectral Ratio of the PL FFO vs free running FFO linewidth



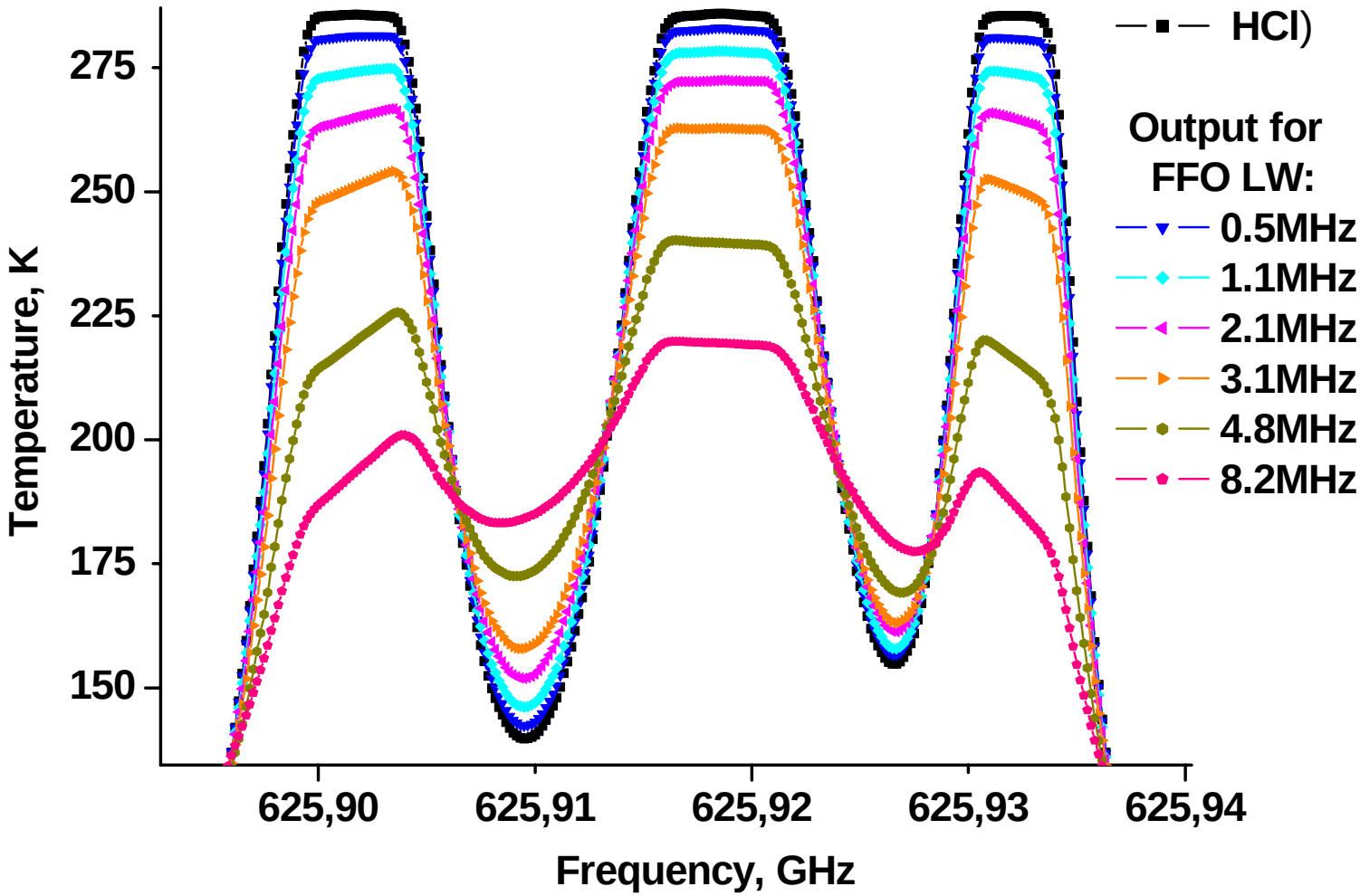
Spectra of the phase-locked and frequency locked FFO + reconstructed PL spectra



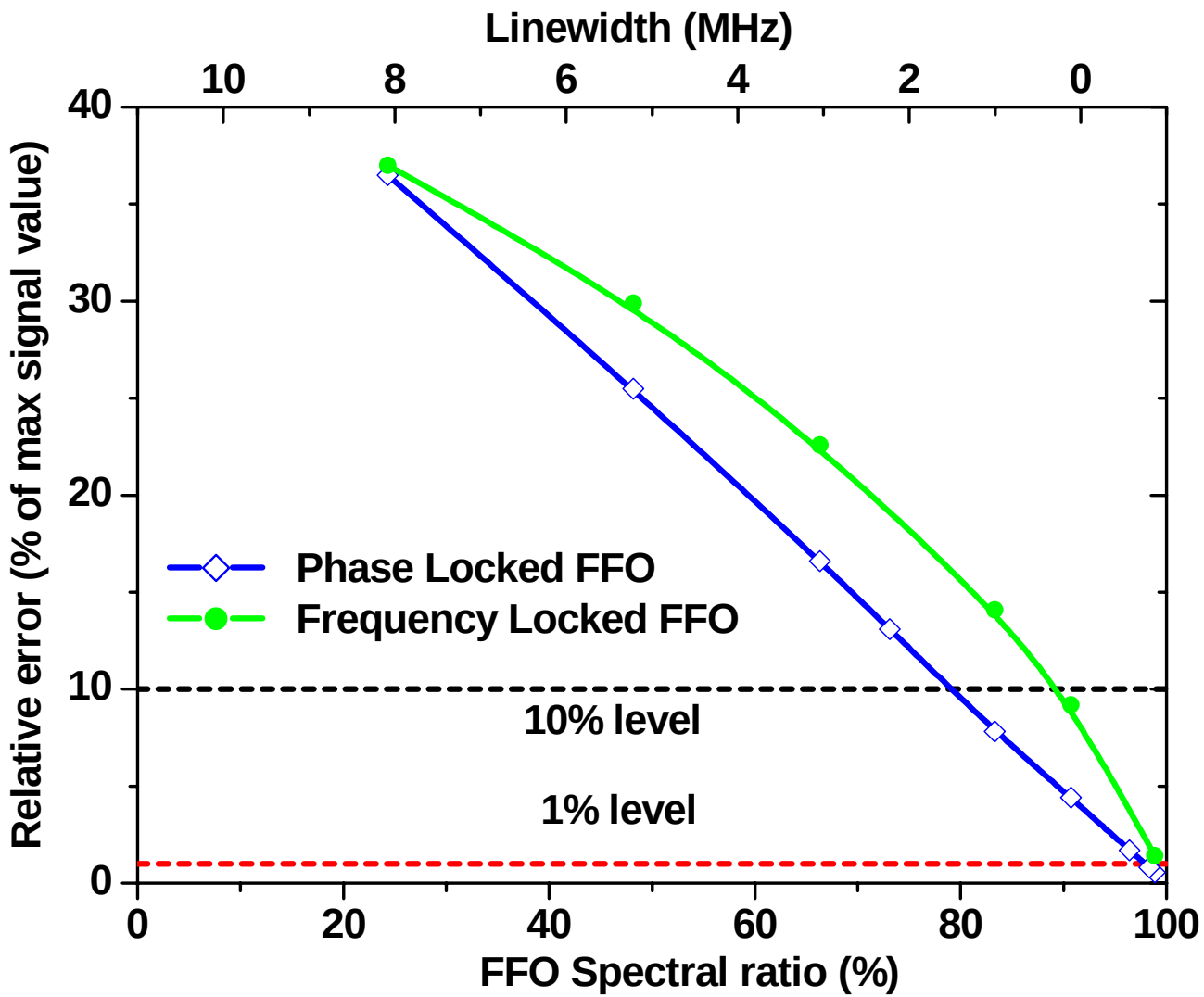
Computer- simulated spectrum of HCl line



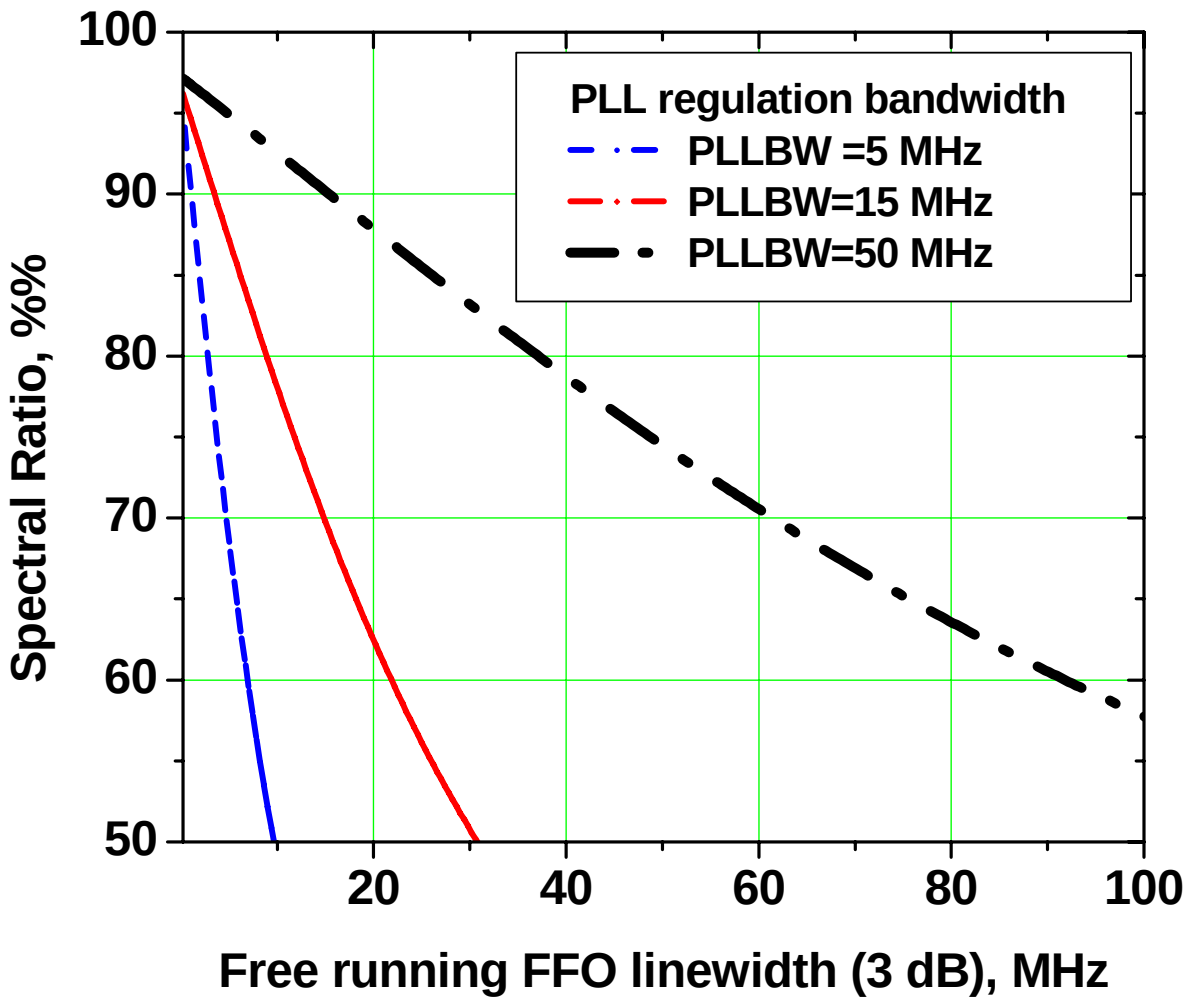
The form of the output spectra at conversion of the HCl line for phase locked FFO



Relative error of conversion of the HCl line



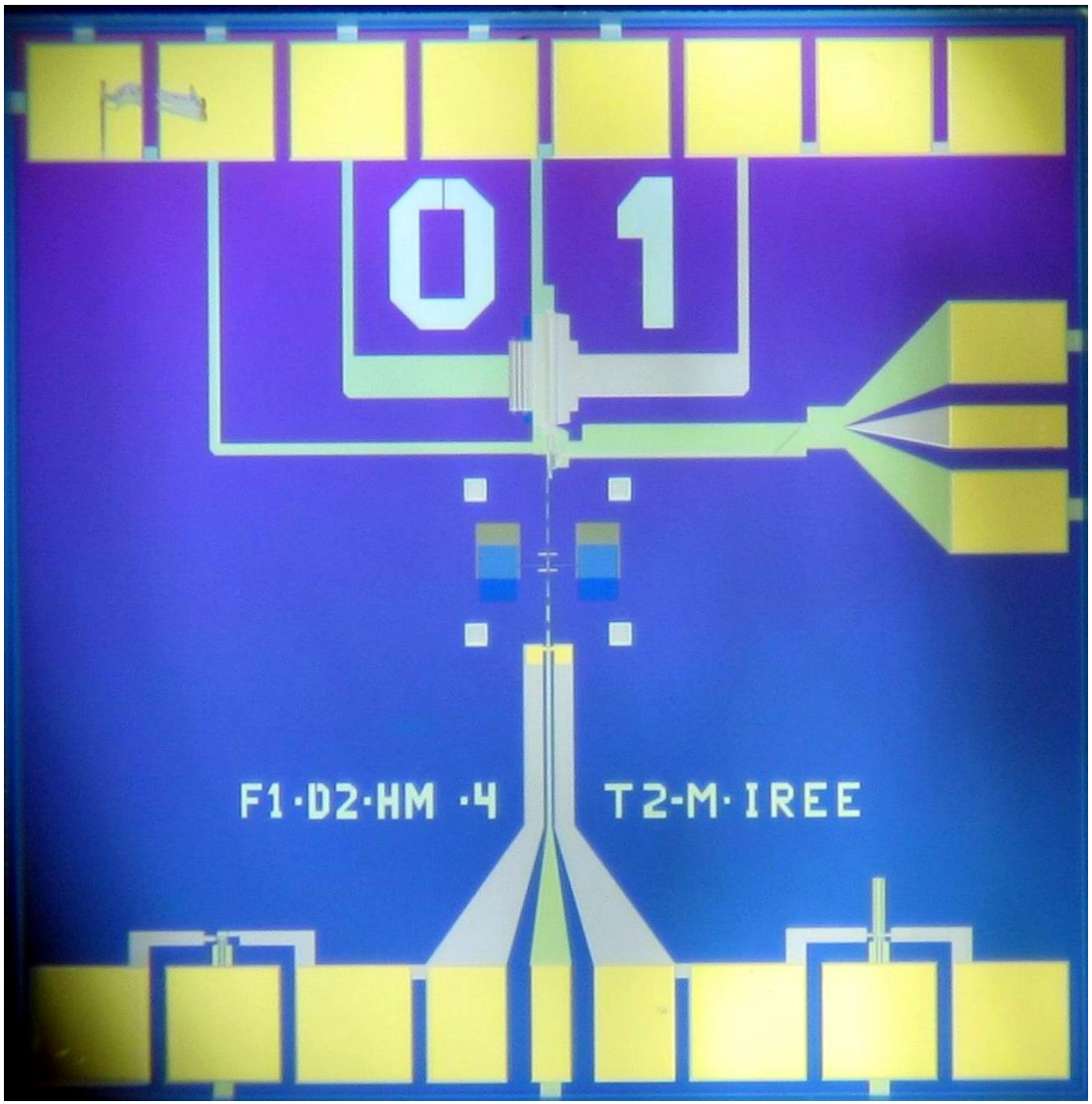
Spectral Ratio vs FFO LW for different PLLBW



PLL BW is limited by length of the cables.

Cryogenic PLL is required!

T2m SIR Microcircuit for TELIS



4 x 4 x 0. 5 mm^3 (Si)

Nb-AlOx-Nb

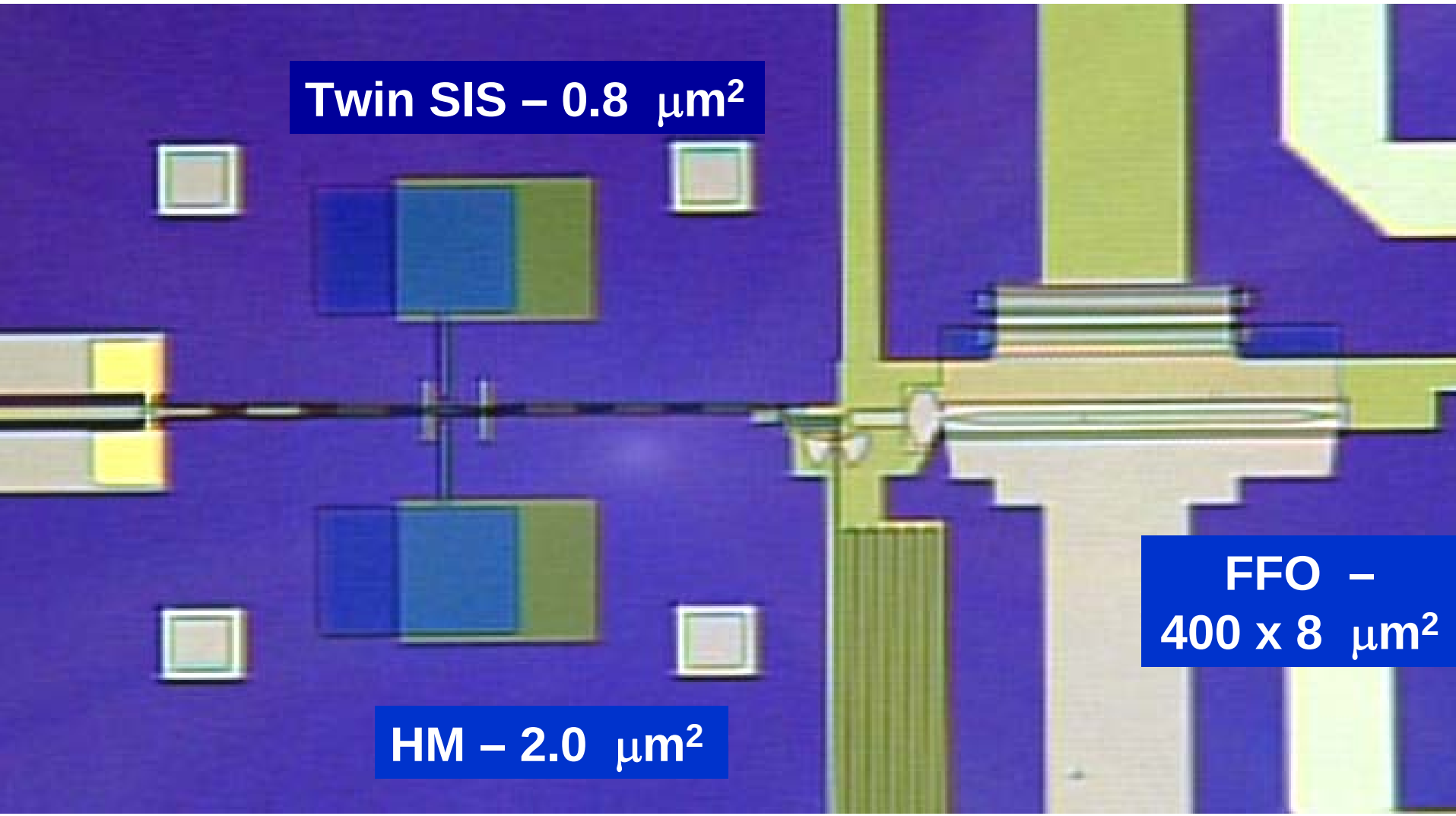
Jc = 8 kA/cm^2

Optionally:

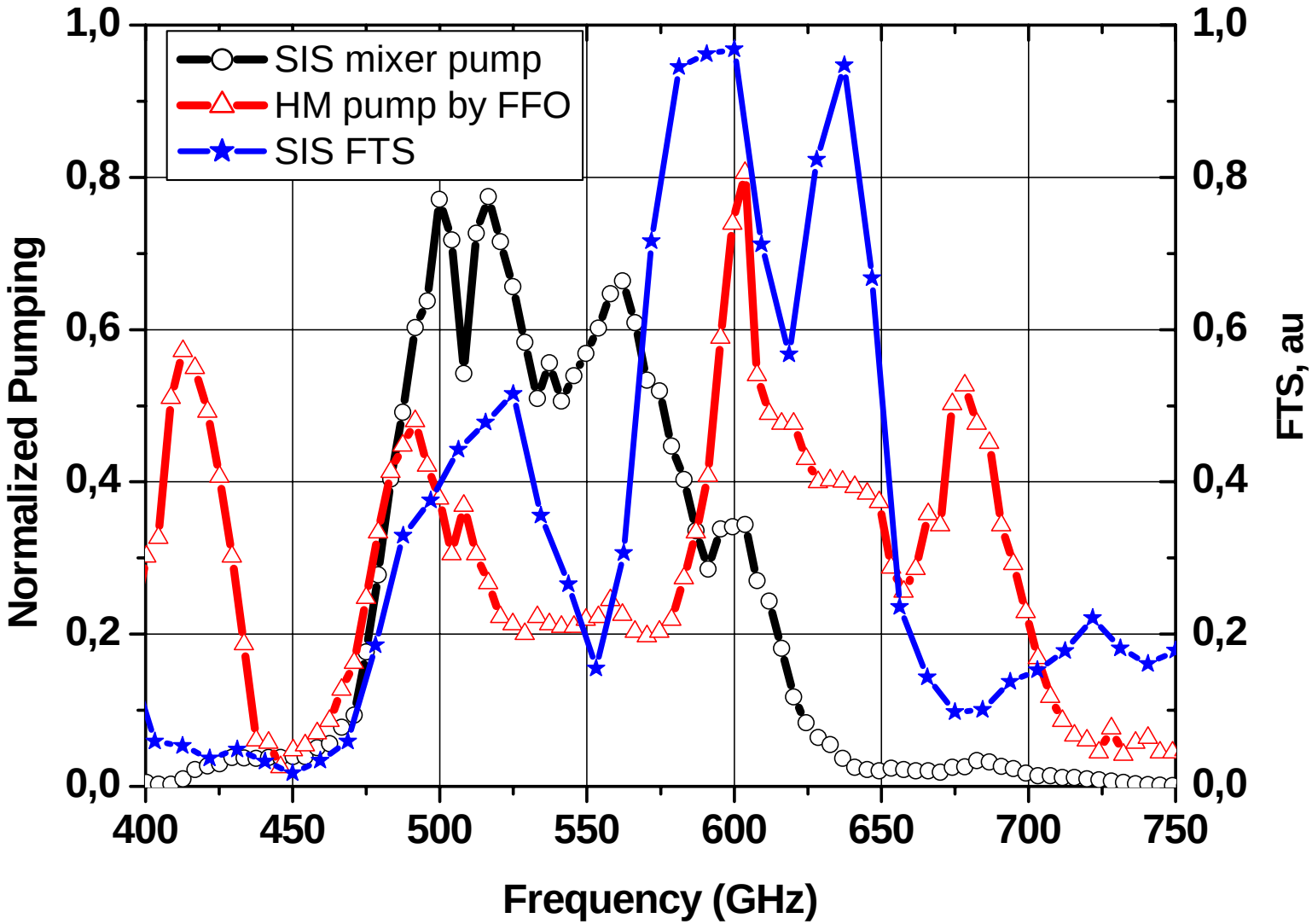
SIS – Jc = 8 kA/cm^2

FFO + HM = 5 kA/cm^2

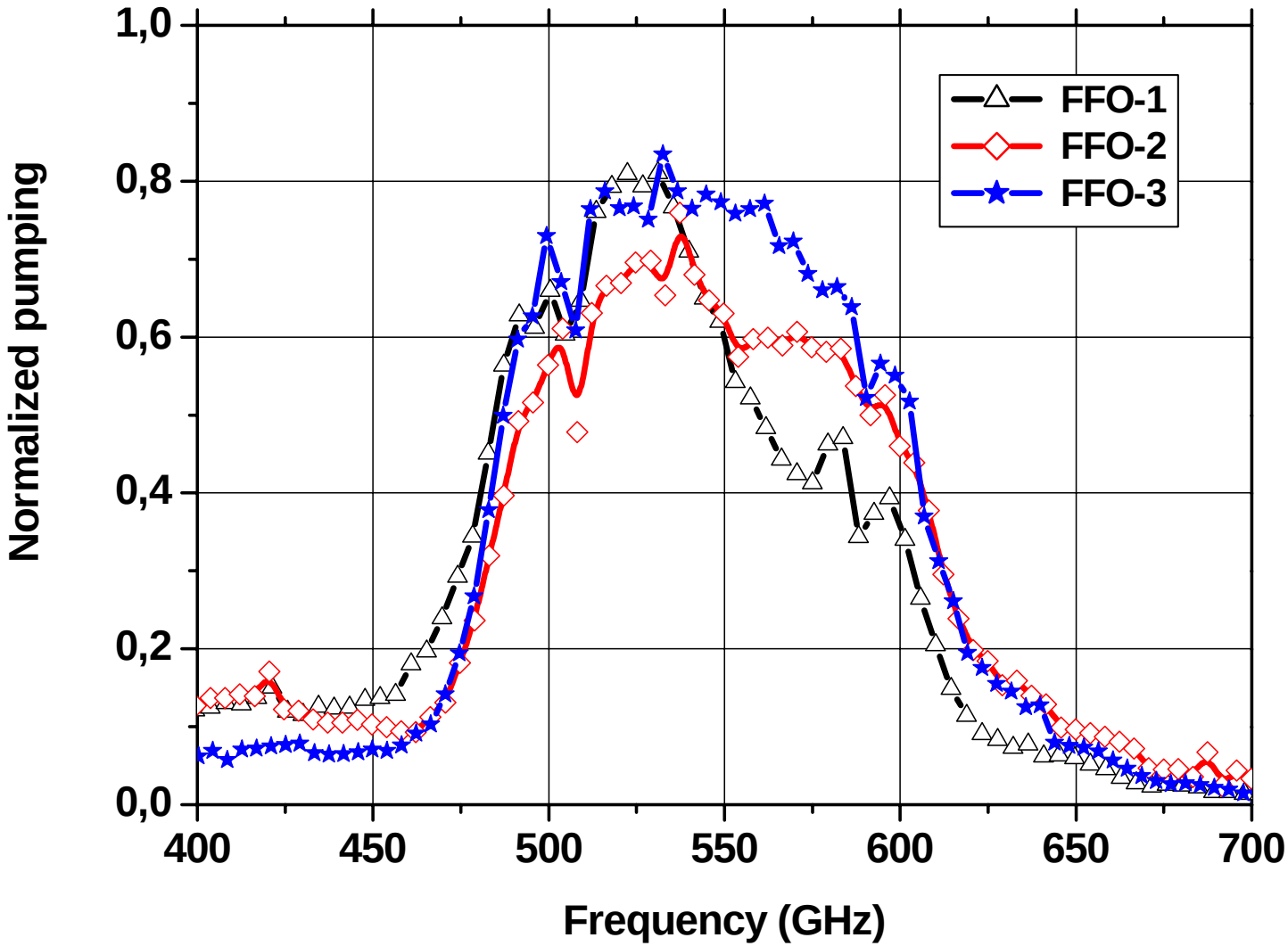
T2m SIR Microcircuit for TELIS



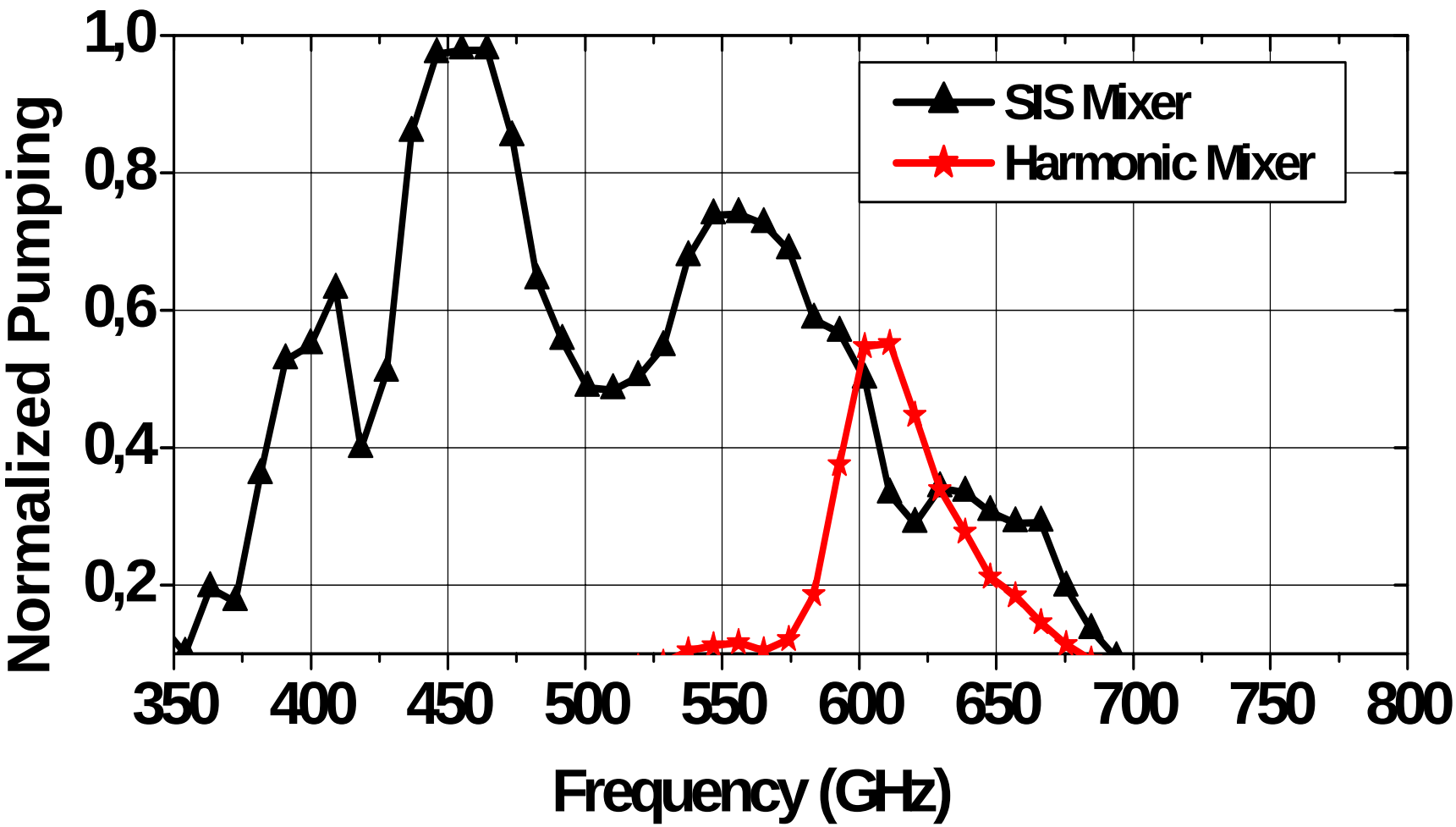
SIS and HM pumping & FTS response for T2m



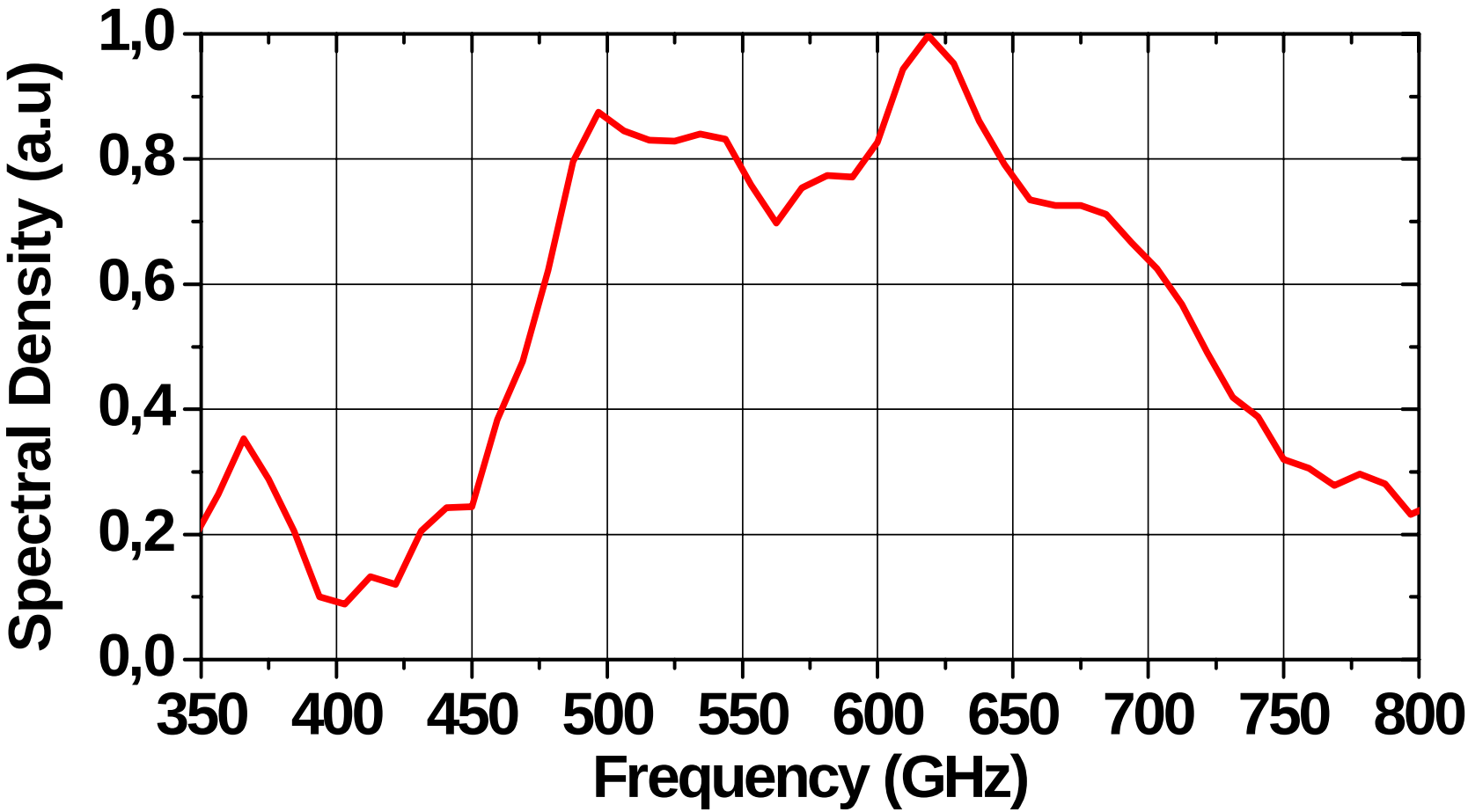
SIS pumping for different T2m FFO designs



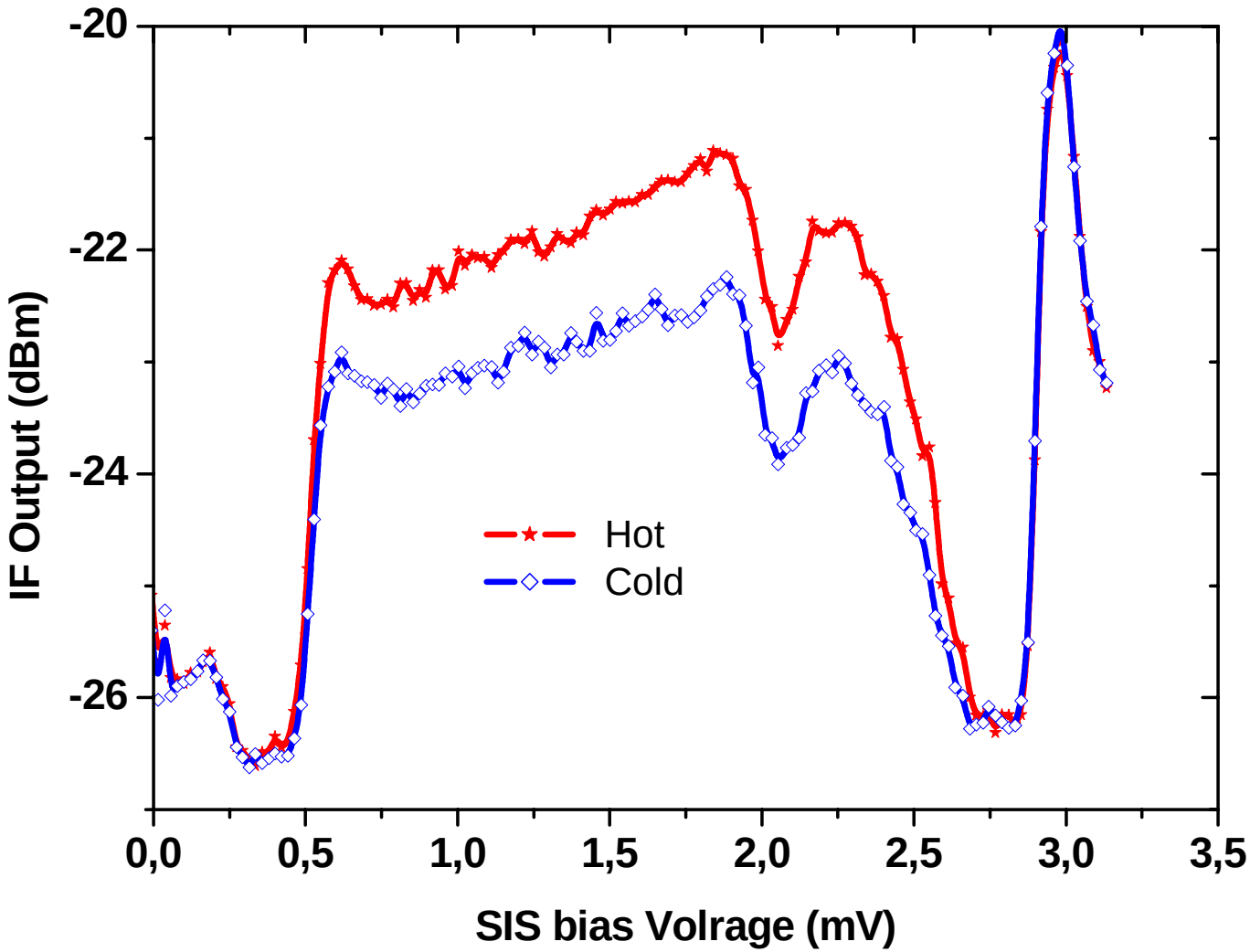
Normalized SIS and HM pumping – T2m, DDA (I_g SIS = 100 μA, I_g HM = 172 μA)



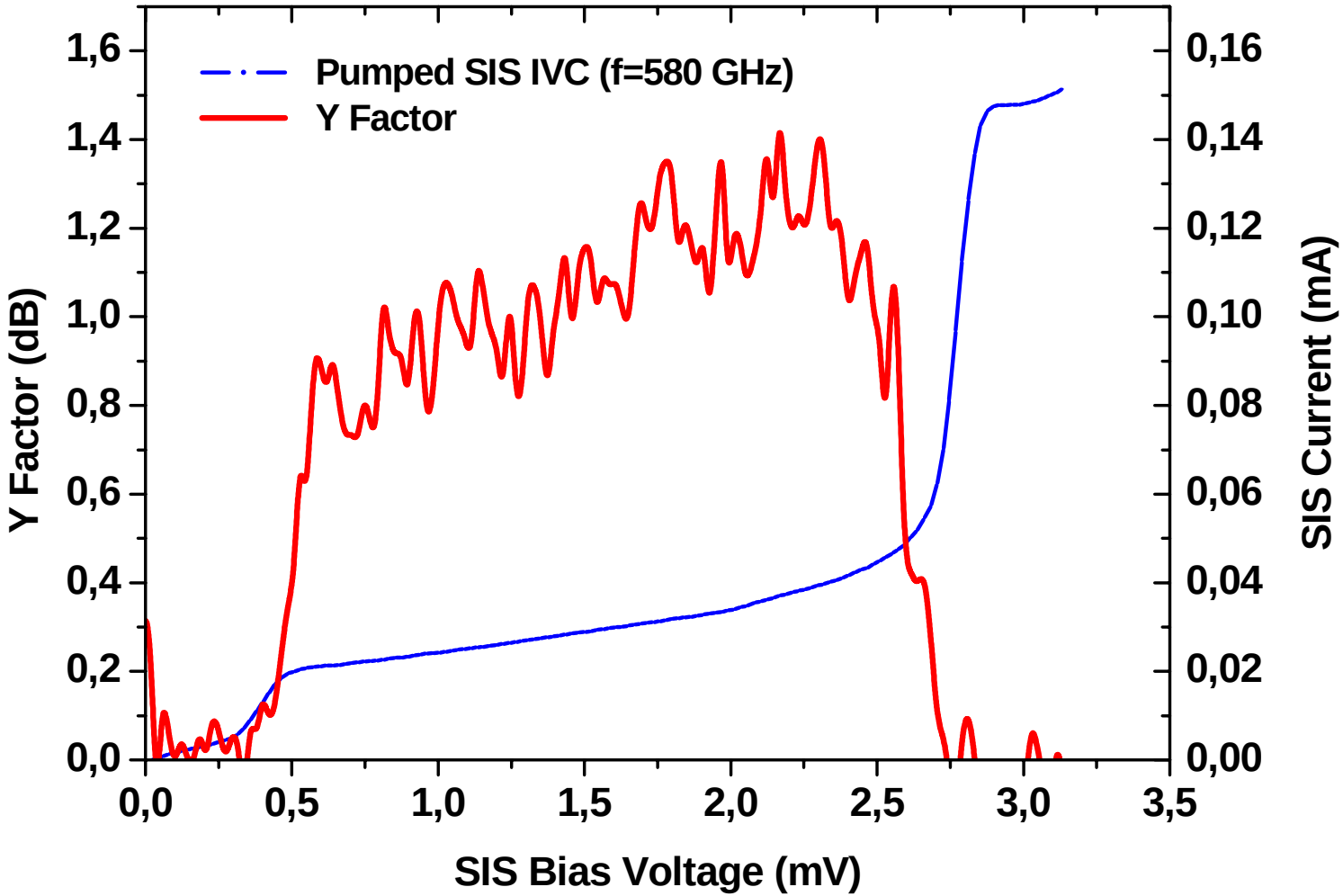
FTS data for double-dipole twin SIS mixer.
A dip at 560 GHz corresponds to water line.



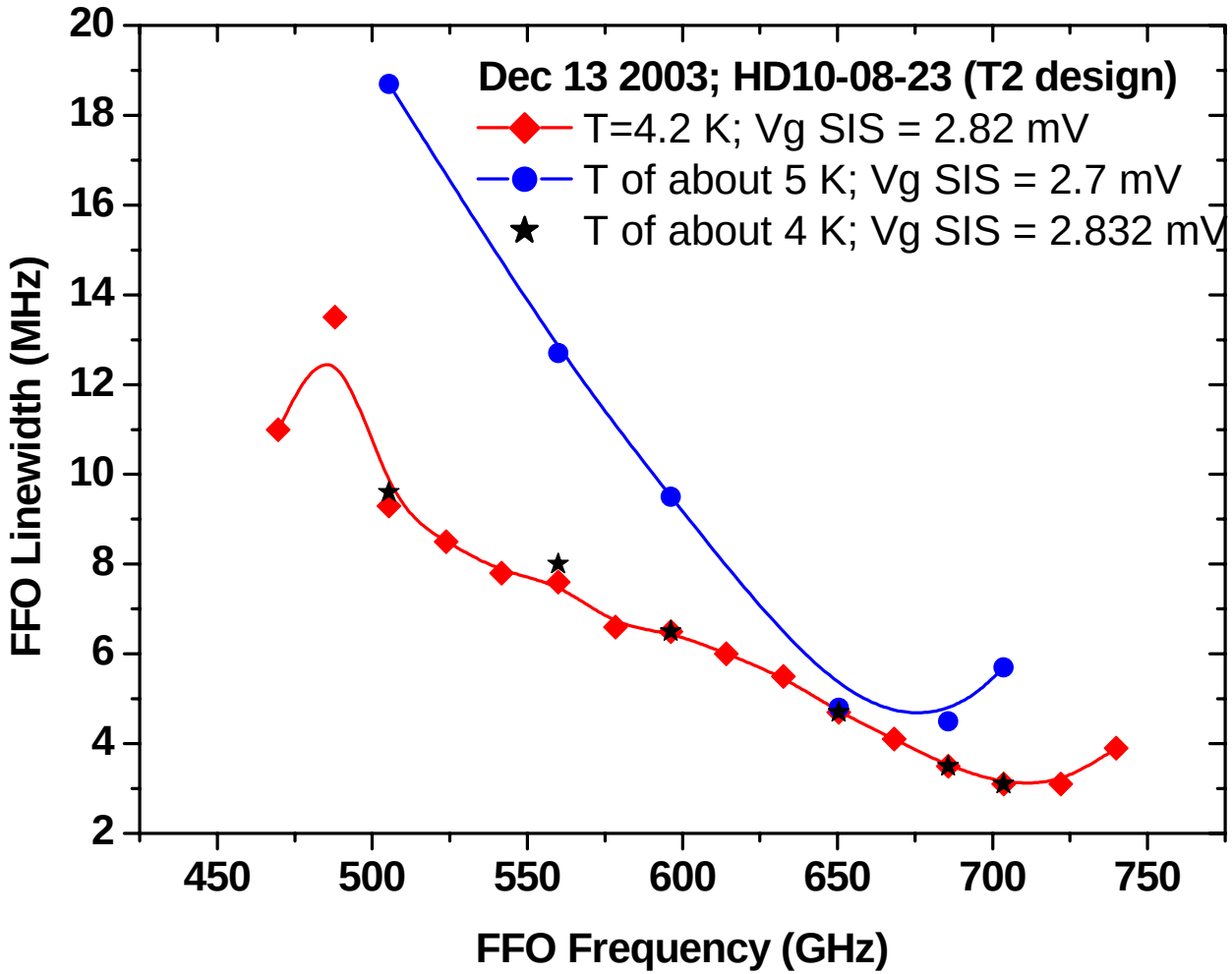
Hot - Cold response for DSA-TM (T2m-031#20c)



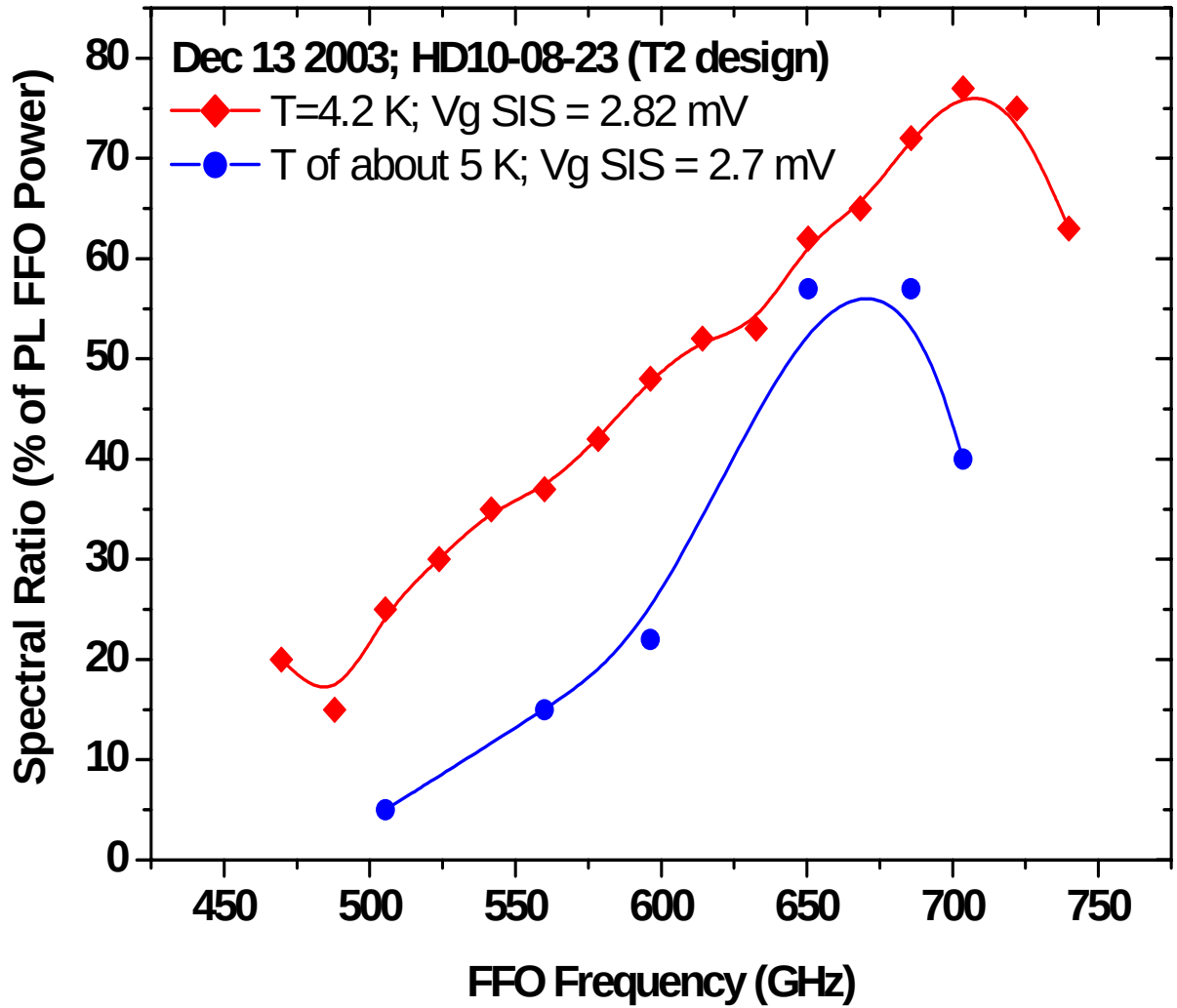
Pumped IVC and Y Factor for T2m-031#20c



FFO linewidth vs FFO frequency, measured at different temperatures



Spectral Ratio of the PL FFO vs frequency, measured at different temperatures



Conclusion (FFO issue)

- Essential dependencies of the FFO linewidth on its frequency, current density and geometry was found;
- Improved design of the FFO for TELIS has been developed and optimized;
- Free-running linewidth from 9 to 2 MHz recorded in the frequency range 500 – 710 GHz (Spectral Ratio of the PL FFO varies from 35 to 87 % correspondingly);
- Free-running linewidth of the FFO below 1 MHz is required to obtain good Spectral Ratio and measure the complicated line profiles with error below 1% (2.5 MHz is the upper limit for 10% error);
- Ultra-wideband cryogenic PLL is needed to realize an ultimate performance of the integrated FFO.

Conclusion (SIR issue)

- Concepts of PL SIR are developed and tested.
- Second generation of the PL SIR IC for TELIS has been developed showing a possibility to realize TELIS requirements.
- Uncorrected receiver DSB noise temperature is of about 500 K at 600 GHz and 630 K at 680 GHz
- Procedure for remote optimization of the PL SIR operation has been developed and experimentally proven.

List of problems and worries (1)

1. Troubles and worries that considerably slow-down the SIR_TELIS measurement and did not allow yet to come to real problems:

1a. Absence of the low-noise computer controlled FFO bias supply;

1b. Limited (almost to zero level) support of electronic and mechanical workshops;

1c. Shortage of Liquid Helium;

1d. Delay in TMM production;

1e. Absence of the licensed software for microwave design and analysis at IREE;

1f. Limited information on scientific requirements of TELIS program (requirements on the LO line shape; most interesting frequencies for TELIS operation).

List of problems and worries (2)

2. Already accounted SIR_TELIS problems:

2a. System complexity problem (N^{α} problem; $\alpha > 2$);

- 2b. Not sufficient cooling of the chip (FFO leakage current);
- 2c. Direct detection of the Hot/Cold load by FFO;
- 2d. Influence of the synthesizer power on the SIS-mixer;
- 2e. TMM design (SIS IF output performance);
- 2f. SIR chip design:
  - Input Bandwidth (FTS) – flatness
    - Range of the FFO/SIS pumping - f > 620 GHz
    - Superfine resonance structure
    - Low Signal to Noise Ratio for HM

List of proposed actions (3) :

3a. (Complexity problem) – Recognition and realization of the task complexity;

3b. (Cooling of the chip) – Joint action: determination of the reasons, additional filters, improved contact of the lens to mixer block, additional cooling straps to chip;

3c. (Direct detection) – Input Band Pass Filters; PLL stabilization of the FFO;

3d. (Influence of Synthesizer on SIS) – Decrease of the HM area down to 1 μm^2, optimization of the TMM design and bonding (ribbon bonding);

3e. (TMM design – IF performance) – Test of originally designed and modified TMM; new TMM design.

3f. (SIR chip design) - Next generations of the SIR chip: modeling, design and test

- T3 - design 12/2004; fabrication 02/2005; test – 05/2005;
- T4 - design 07/2004; fabrication 10/2005; test – 12/2005;
- T5 - design 06/2006; fabrication 09/2006; test – 12/2006;