Status of the SIR program for TELIS

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Status of the SIR program for TELIS

Outline

• TELIS requirements for SIR channel. Concepts of PL SIR for TELIS
• Design of SIR for TELIS
• FFO for TELIS, PL operation
• Optimization of HM design and regimes
• Computer control of SIR operation
• First test results of T2 SIR
• Conclusion
# Main parameters of TELIS-SIR spectrometer

<table>
<thead>
<tr>
<th>##</th>
<th>Description</th>
<th>Base line</th>
<th>Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input frequency range, GHz</td>
<td>600 - 650</td>
<td>500-650</td>
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<tr>
<td>2</td>
<td>Minimum noise temperature in the range (DSB), K</td>
<td>200</td>
<td>250</td>
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<tr>
<td>3</td>
<td>Output IF range, GHz</td>
<td>5 - 7</td>
<td>4 - 8</td>
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<tr>
<td>4</td>
<td>Spectral resolution, MHz</td>
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<td>1</td>
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<tr>
<td>5</td>
<td>Contribution to the nearest spectral channel by phased locked FFO (dynamic range), dB</td>
<td>-20</td>
<td>-20</td>
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<tr>
<td>6</td>
<td>Contribution to a spectral channel by phased locked FFO at 4-8 GHz offset from the carrier, K</td>
<td>20</td>
<td>20</td>
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<tr>
<td>7</td>
<td>LO frequency net (distance between nearest settings of the PL FFO frequency), MHz</td>
<td>&lt; 300</td>
<td>&lt; 300</td>
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<tr>
<td>8</td>
<td>Dissipated power at 4.2 K stage (including IF amplifiers chain), mW</td>
<td>100</td>
<td>50</td>
</tr>
<tr>
<td>9</td>
<td>Operation temperature, K</td>
<td>&lt; 4.5</td>
<td>&lt; 4.5</td>
</tr>
</tbody>
</table>
Requirements for TELIS-SIR spectrometer

- **5** – required dynamic range of the spectrometer - 20 dB. It corresponds to PL FFO Phase Noise –80 dBC/Hz at the 1 MHz offset from the carrier.

- What about remote channels (10 –100 MHz offset)? Do we need “1/f reduction” as required for WBS-HIFI? That corresponds to -100 dBC/Hz at 10 MHz offset!!

- **6** Contribution to a spectral channel by phased locked FFO at 4-8 GHz offset from the carrier should be < 10% of SIR Tr (< 20 K). It corresponds to:
  \[ NCR = 10 \log (T_{LO} * k_B) - 10 \log (P_{LO}^{opt}) = -152 \text{ dBc/Hz} \]

- An additional argument for balanced integrated receiver!
Phase Noise of the PL FFO

- • Phase locked FFO, $f_{FFO} = 707.45$ GHz ($\delta f_{aut} = 6.3$ MHz)
- • Phase locked FFO, $f_{FFO} = 450$ GHz ($\delta f_{aut} = 0.5$ MHz)
- • HP Synthesizer at 18 GHz $\times n^2$ ($n = 24$)
- • HIFI Specifications for 24 - 35 GHz Synthesizer

Absolute FFO phase noise, $f_{FFO} = 450$ GHz ($n = 24$)
Absolute FFO phase noise, $f_{FFO} = 707.45$ GHz ($n = 39$)
HP Synthesizer at 18 GHz

Phase Noise (dBc/Hz)

Offset from Carrier (Hz)
3 Concepts of a SIR with PL FFO

Liquid Helium

T=4.2K

Beam Splitter

Optical Input

Harmonic Multiplier (T=4.2 K)

IF-1 4-8GHz (T=4.2K)

SIS Mixer with antenna

FFO

Directional Coupler (T=4.2 K)

IF-1 4-8GHz (T=4.2 K)

IF Filter 3.7-4.3GHz

LO=3.6GHz

Down Converter

PLL Circuit

Ref = 400 MHz

LO = 3.6 GHz

10 MHz Reference

LSU 22-24 GHz

Back End
Challenges in SIR Design: Requirements

- **500-650 GHz SIS mixer**
  - SSB Trx < 250 K @ 600-650 GHz
  - Twin-SIS is the most suitable solution

- **Wide-band IF (4-8 GHz) coupling circuit**
  - High capacitance of the structure

- **LO match & Integration of PLL circuit**
  - FFO operates above the boundary voltage
  - Exact power split at the antenna-mixer
  - Minimum power for HM
  - External harmonic generator as a safe option
Design Novelties: 3-D EM Modeling

Double-Slot Antenna (DSA) Mixer
Mask Set T2: Wafer Layout
Mask Set T2: SIR DDA Chip Layout
Mask Set T2: DDA Layout (magnified)
Mask Set T2: SIR DSA Chip Layout
Mask Set T2: Reference Chip Layout
Numerical Simulations: Single-SIS DDA Mixer

S R1 Mixer

Coupling (dB)

Frequency (GHz)

500 550 600 650 700 750

-10 -8 -6 -4 -2 0

670 GHz -3

571 GHz -3
Numerical Simulations: Twin-SIS DDA Mixer

Mixer Coupling

Frequency (GHz)

Coupling (dB)

521 GHz
-3
Numerical Simulations: Twin-SIS DSA Mixer

Reference Twin-SIS Mixer

Coupling (dB)

Frequency (GHz)
Numerical Simulations:
IF Connection of the Chip
Numerical Simulations: IF Connection of the Chip

Single-SIS Coupling at IF
FFO for TELIS (Outline)

• FFO power (dependence on design)
• FFO linewidth (dependence on design, FFO frequency and current density)
• FFO for T-2
• PLL results
• FFO IVCs reproducibility, other issues
• Conclusion
**Calculated IVCs of SIS mixer at different levels of power, delivered to mixer at 500 GHz**

\[
\begin{align*}
\text{Idc}(V_n) \cdot 10^6 \\
\text{Ip}(V_n, 1) \cdot 10^6 \\
\text{Ip}(V_n, 2.6) \cdot 10^6 \\
\text{Ip}(V_n, 4) \cdot 10^6 \\
\end{align*}
\]

- \( R_n = 15 \, \Omega \)
- \( R_nS = 30 \, \Omega \cdot \mu^2 \)

- 0.74 \, \mu W
- 1.1 \, \mu W
- 0.25 \, \mu W

08 April

SIR for TELIS
Dependence of the current on photon induced step on power

\[ R_n = 15 \, \Omega; \quad R_nS = 30 \, \Omega^* \mu^2; \quad f = 500 \, \text{GHz}; \quad V_{sis} = 2.5 \, \text{mV} \]

\[ \alpha = \frac{eV_{rf}}{hf} \]

\[ \alpha = 1 - \text{optimal pumping} \]
(corresponds to 0.25 \( \mu \text{W} \) for listed above SIS parameters)
HD7-09#02 (RnS = 26 Ω*μ²)
SIS Pumping by FFO (HD7 & T1 design)

\[ \text{SIS I pump (normalized on } I_g) \]

- \( \text{RnS} = 50 \, \Omega \cdot \mu m^2 \)
- \( \text{RnS} = 34 \, \Omega \cdot \mu m^2 \)
- \( \text{RnS} = 26 \, \Omega \cdot \mu m^2 \)
- \( \text{RnS} = 19 \, \Omega \cdot \mu m^2 \)
- \( \text{RnS} = 11 \, \Omega \cdot \mu m^2 \)

\[ \text{FFO Frequency (GHz)} \]

---

08 April SIR for TELIS 23
New FFO design HD9 with distributed bias
HD9-04#13 (RnS = 37 $\Omega\mu^2$)

(#HD9-04#13c.06-08-2003) $\lg SIS = 85$ uA

SIS Ipump (uA)

FFO Frequency (GHz)
HD9-03-04 (RnS = 27.5 $\Omega*\mu^2$)

(#HD9-03#04.05-26-2003) \( \lg SIS = 157 \, \mu A \)
FFO IVCs - HD9-03-04 (RnS = 27.5 Ω·µ²)
HD9-03#04; SIS pumped by FFO RnS = 27.5 Ω*μ²

(#HD9-03#04.05-26-2003)(Rn=14.63 Rj/Rn=18.4 Vg.mV=2.79)
SIS Pumping by FFO (Different Designs)

![SIS Pumping by FFO (Different Designs)](image)

- HD6 RnS = 50 $\Omega \mu m^2$
- HD6 RnS = 26.5 $\Omega \mu m^2$
- HD6 RnS = 15 $\Omega \mu m^2$
- HD9 RnS = 37 $\Omega \mu m^2$
- HD6 RnS = 27.5 $\Omega \mu m^2$
- HD7 RnS = 26 $\Omega \mu m^2$

Linear Fit on HD6-HD9 Data
FFO Power delivered to HM and SIS mixer

• Analysis of the results for different FFO designs (including FFO used in T1), which were fabricated with various current density (RnS) has demonstrated that delivered to HM power depends both on FFO design and junctions’ RnS.

• Reason of insufficient pumping for T1 circuits at high frequencies and high current density has been found.

• New designs for T2 have been developed and tested, these circuits demonstrate sufficient pumping from 250 to 700 GHz for RnS from 50 to 15 Ω*μ².
FFO Linewidth: Dependence on FFO Frequency and Current Density

![Graph showing FFO Linewidth vs. FFO Frequency for different current densities.]

- Jc=8.5kA/cm², Ib=15mA
- Jc=5.8kA/cm², Ib=11mA
- Jc=4.2kA/cm², Ib=12mA
IVCs of FFO measured at different Icl

\[ R_d^B = \frac{\partial V}{\partial I_B} \]
\[ R_d^{CL} = \frac{\partial V_{FFO}}{\partial I_{CL}} \]
$R_d^{CL}$ as a function of $R_d$

$$R_{dCL} = 0.001 + 2.73*R_d$$

$I_b = 30\ mA$

$I_b = 27\ mA$

$I_b = 21\ mA$

$I_b = 15\ mA$
FFO Linewidth: Dependence on FFO Voltage and Current Density

![Graph showing FFO Linewidth vs. FFO Frequency]

- $J_c = 8.5 \text{kA/cm}^2$, $I_b = 15 \text{mA}$
- $J_c = 5.8 \text{kA/cm}^2$, $I_b = 11 \text{mA}$
- $J_c = 4.2 \text{kA/cm}^2$, $I_b = 12 \text{mA}$

Free-running FFO Linewidth (MHz) vs. FFO Frequency (GHz)
Normalized FFO Linewidth

\[
\Delta f := \left(\frac{2 \cdot e}{h}\right)^2 \cdot \left(R_d + K \cdot R_{dCL}\right)^2 \cdot \left(\frac{e \cdot (I_{qp})}{2 \cdot \pi} \cdot \coth\left(\frac{e \cdot V}{2 \cdot k_b \cdot T}\right) + \frac{2 \cdot e \cdot (I_s)}{2 \cdot \pi} \cdot \coth\left(\frac{e \cdot V}{k_b \cdot T}\right)\right) + \frac{1}{\pi} \cdot \left(\frac{2 \cdot e}{h}\right) \cdot (R_d + R_{dCL}) \cdot I_{lf}
\]

\[
\begin{aligned}
J_c = 8.5 \text{ kA/cm}^2; & \quad K = 0.25 \\
J_c = 5.8 \text{ kA/cm}^2; & \quad K = 0.15 \\
J_c = 4.2 \text{ kA/cm}^2; & \quad K = 0.0
\end{aligned}
\]
\[ \Delta f := \left( \frac{2 \cdot e}{h} \right)^2 \cdot (R_d + K \cdot R_{dCL})^2 \cdot \left[ \frac{e \cdot (lqp)}{2 \cdot \pi} \cdot \coth \left( \frac{e \cdot V}{2 \cdot k_b \cdot T} \right) + \frac{2 \cdot e \cdot (lsp)}{2 \cdot \pi} \cdot \coth \left( \frac{e \cdot V}{k_b \cdot T} \right) \right] + \frac{1}{\pi} \cdot \left( \frac{2 \cdot e}{h} \right) \cdot (R_d + R_{dCL}) \cdot I_{lf} \]

**Normalized FFO Linewidth**

![Graph showing normalized FFO linewidth vs. FFO frequency (GHz) for different junction currents (Jc) and interaction constants (K).](image-url)
FFO Linewidth on \((R_d + R_d^{CL})\)

- \(R_{nS} = 26; I_b = 26\) mA
- \(R_{nS} = 50; I_b = 5\) mA
- \(R_{nS} = 50; I_b = 10\) mA
- Theory \(I_b = 26\) mA; \(K = 0.15; I_{fl} = 85\) nA
- Theory \(I_b = 5\) mA; \(K = 0.37; I_{fl} = 13\) nA
FFO Linewidth (Design issue)

- $J_c = 5.8 \text{kA/cm}^2$
- Traditional design
- 20 biasing "fingers"
- 13 biasing "fingers"
- "unbiased tail"

Graph showing the relationship between FFO free-running LW (MHz) and FFO frequency (GHz) with different biasing configurations.
FFO of T2 design with unbiased tail
Spectral Ratio of the PL FFO vs free running FFO linewidth

![Graph showing the relationship between spectral ratio and free-running FFO linewidth. The y-axis represents the spectral ratio (% of PL FFO Power) ranging from 0 to 100, and the x-axis represents the free-running FFO linewidth (MHz) ranging from 0 to 14. The graph includes data points from December 2003; T2 design and June 06 2003; HD6-05-05.]
Spectral Ratio of the PL FFO vs free running FFO linewidth

![Graph showing spectral ratio (%) of PL FFO power vs free-running FFO linewidth (MHz). The graph includes data points from Dec 2003; T2 design and June 06 2003; HD6-05-05.]
FFO LW and SR vs FFO frequency

\( W_{\text{FFO}} = 10 \mu; \quad RnS = 40 \Omega^* \mu^2 \)
Phase Noise of the PL FFO (Breadboard)

- Phase locked FFO, $f_{\text{FFO}} = 680 \text{ GHz}$ ($\delta f_{\text{aut}} = 11 \text{ MHz}; \text{SR} = 0.3$)
- Phase locked FFO, $f_{\text{FFO}} = 450 \text{ GHz}$ ($\delta f_{\text{aut}} = 3.8 \text{ MHz}; \text{SR} = 0.8$)
- HP Synthesizer at $18 \text{ GHz} \times n^2$ ($n = 25$)
- Absolute FFO phase noise, $f_{\text{FFO}} = 450 \text{ GHz}$ ($n = 25$)
- Absolute FFO phase noise, $f_{\text{FFO}} = 680 \text{ GHz}$ ($n = 38$)
- HP Synthesizer at $18 \text{ GHz}$
- TELIS LSU Spec
FFO linewidth vs FFO frequency, measured at different temperatures

- Dec 13 2003; HD10-08-23 (T2 design)
  - T=4.2 K; Vg SIS = 2.82 mV
  - T of about 5 K; Vg SIS = 2.7 mV
  - T of about 4 K; Vg SIS = 2.832 mV
Spectral Ratio of the PL FFO vs frequency, measured at different temperatures

Dec 13 2003; HD10-08-23 (T2 design)
- T=4.2 K; Vg SIS = 2.82 mV
- T of about 5 K; Vg SIS = 2.7 mV
FFO Shielding

- Superconducting shield: stability of the PL FFO at changing of dewar orientation.
- Magnetic / Superconducting shield combination: reproducibility of the FFO state after heating.
Free-running and PL FFO Spectra; $f_{FFO} = 687$ GHz
Free-running and PL FFO Spectra, dewar rotated on 90 deg

<table>
<thead>
<tr>
<th>Time</th>
<th>Center: 400.0MHz</th>
<th>Span: 100.0MHz</th>
<th>Points</th>
</tr>
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<tbody>
<tr>
<td>06/04/03 10:49:56 PM</td>
<td></td>
<td></td>
<td>601 pts</td>
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</tbody>
</table>

**Trace A**
- Log 5.00 dB/div
- Ref 0.000 dBm

**Trace B**
- Log 5.00 dB/div
- Ref 0.000 dBm

Center: 400.00 MHz
Span: 100.00 MHz
RBW 1.0 MHz
VBW 30.0 kHz
Sweep Time: 50.00 msec
AT 10 dB
Normal
Free-running and PL FFO spectra, dewar rotated on - 90 deg
FFO IVCs measured after 2 consequent thermocyclings (‘usual” situation – there is a shift of about 100 \( \mu \)V)
Part of the FFO IVCs measured after 3 consequent thermocyclings (‘perfect’ situation – shift is of about 1 µV)
SIS IVCs pumped by FFO measured after 2 consequent thermocyclings

(#HD9-04#17c, 07-08-2003) \( R_n = 27.77 \) \( R_j/R_n = 16.9 \) \( V_g, mV = 2.79 \)
2-D diagram for HM operational parameters measured by PC controlled PLL. The color represents the IF-out PLL signal.
3-D diagram for HM operational parameters measured by PC controlled PLL. The color represents the IF-out PLL signal.
Dependence of the PLL_IF level on HM bias voltage at 2 values of synthesizer power (13.25 dBm – red and 8.5 dBm – blue)
Dependence of the PLL_IF level on synthesizer power at HM bias voltage = 0.0 mV.
Dependence of the PLL_IF level on the PLL Gain setting

(#HD11-01#25c,03-16-2004)
Algorithms for TSCU (block diagram)

1. **Test of TSCU electronics**
   - Ic (HM) > level?
     - Yes: Check SIS mixer and FFO
     - No: Set frequency and power of the synthesizer

2. **Measure offsets**
   - Is frequency in the range?
     - Yes: Set FFO, SIS mixer (from data chart)
     - No: Fine adjust FFO frequency by FFO CL
   - HC
     - No: Yes
     - Yes: Adjust SIS pump-level by FFO BIAS & FFO BIAS CL at the same frequency

3. **Heating chip (HC)**
   - Is SIS Ipump in the range?
     - Yes: Optimize IF signal by power of synthesizer and HM SIS voltage in narrow ranges
     - No: Fine tune FD & PD signal by FFO CL
   - HC
     - No
     - Yes

4. **Turn on frequency detector (FD)**
   - FD signal?
     - Yes: Scan FFO frequency by FFO CL in narrow range
     - No (signal is absent): Set FFO, SIS mixer (from data chart)
     - No:

5. **PD signal?**
   - Yes: Accept measurement
   - No: Yes
     - FD & PD < level?
       - Yes: Fine tune FD & PD signal by FFO CL
       - No: Accept measurement

6. **Turn on phase lock**
   - Check & adjust frequency
   - Monitoring and check FD & PD

---

Feedback and suggestions are welcome!
# Table of available T2 SIR batches

<table>
<thead>
<tr>
<th>#</th>
<th>Date</th>
<th>Substrate</th>
<th>RnS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2011</td>
<td>20/10/2003-25/10/2003</td>
<td>Si 300 μm, one side polished</td>
<td>28-30</td>
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<td>T2012</td>
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</tr>
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<td>T2021</td>
<td>27/10/2003-6/11/2003</td>
<td>Si 300 μm, one side polished</td>
<td>28-30</td>
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<td>T2022</td>
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<td></td>
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</tr>
<tr>
<td>T2031</td>
<td>31/10/2003-12/11/2003</td>
<td>Si 300 μm one side polished</td>
<td>28-30</td>
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<td>T2032</td>
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<tr>
<td>T2041</td>
<td>13/10/2003-20/10/2003</td>
<td>Si 520 μm, two side polished</td>
<td>28-30</td>
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<tr>
<td>T2051</td>
<td>13/10/2003-20/10/2003</td>
<td>Si 520 μm, two side polished</td>
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<td>T2052</td>
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<tr>
<td>T2061</td>
<td>20/01/2004-30/01/2004</td>
<td>Si 520 μm, two side polished</td>
<td>20-24</td>
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<td>T2062</td>
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<td>T2071</td>
<td>20/01/2004-30/01/2004</td>
<td>Si 520 μm, two side polished</td>
<td>15-17</td>
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<td>T2072</td>
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<tr>
<td>T2081</td>
<td>9/02/2004-20/02/2004</td>
<td>Si 520 μm, two side polished</td>
<td>15-17</td>
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<tr>
<td>T2082</td>
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Dipstick Tests: Twin-SIS Mixer Pump Level

\[ f = 613 \text{ GHz} \]
Dipstick Test: FFO Power Range
Dipstick Test: FFO Power Range

SIS pump ref. level (mA) = 0.065

Frequency (GHz)

470  549.389  650
FTS Test: DDA Single-SIS Mixer

FTS Response of Single-SIS DDA Mixer T201111B
FTS Test: **DDA Twin-SIS Mixer**

FTS Response of Twin-SIS DDA Mixer T202111R

![Graph showing detected spectral density versus frequency](image)
FTS Test: DSA Twin-SIS Mixer

FTS Response for Twin-SIS DSA Mixer T202111T

![Graph showing frequency vs. detected spectral density for Twin-SIS DSA Mixer T202111T. The graph has a red line with peaks and valleys indicating the response across different frequencies. The frequency range is from 400 GHz to 800 GHz, and the detected spectral density range is from 0 to 1 unit of measure (a.u.).]
Simulation vs. Test: 
Pump of Harmonic Mixer

550 GHz 
-12.4 dB

615 GHz 
-18.9 dB

695 GHz 
-3.96 dB
Test: brief arrangement of new cryostat

Preliminary Noise Breakdown

- Y-factor 1-1.3 dB @ 600-630 GHz
- 50 μm beam splitter (BS) transparent 65% @600 GHz; T_{cold} rises from 80 K to 156 K
- TRX corrected for BS is 250-380 K
- Dewar window & two infrared filters T = 50%
- IF coupling -2.5 dB @ IF=1.5 GHz
- Final estimate 100-120 K (DSB)
- NOTE: Cooling might be insufficient
Test Summary

- **Production of circuits is going satisfactory**
  - Reproducible small area (0.8 \( \mu \text{m}^2 \)) SIS junctions

- **Twin SIS covers band 520-680 GHz**
  - Flat response has been achieved

- **Single-SIS as a narrow-band option**
  - Single-SIS is OK for band 600-650 GHz

- **Noise Temperature Preliminary Estimate**
  - Known corrections give 120K (DSB) at IF=1.5 GHz
T2 chips selected for further receiver test

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Type</th>
<th>Expected full performance band (GHz)</th>
<th>FTS band (GHz)</th>
<th>$R_W$ SIS / HM (Ω)</th>
<th>$Q$ Rj/Rn a.u.</th>
<th>$I_{CL}$ zeroing (mA)</th>
<th>Pump range $f_1$-$f_2$ of SIS / HM (GHz)</th>
<th>$I_{step\ max}$ (mA)</th>
<th>$I_{CL\ FFO\ range}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T204102</td>
<td>F1-S2-HM-4</td>
<td>570-650</td>
<td>490-520,570-800</td>
<td>22.4/11.8</td>
<td>26/23</td>
<td>89</td>
<td>550-700/550-650</td>
<td>37</td>
<td>22-33</td>
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<td>T201105</td>
<td>F1-D2-HM-4</td>
<td>600-625</td>
<td>600-700</td>
<td>9.56/4.11</td>
<td>14/23</td>
<td>19-55-80</td>
<td>480-630/620-670</td>
<td>32</td>
<td>25-29</td>
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<td>T201103</td>
<td>F2-D2-HM-4</td>
<td>500-550,580-630</td>
<td>470-700</td>
<td>8.61/5.41</td>
<td>26/7</td>
<td>34-68-88</td>
<td>470-630/520-700</td>
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<td>15-23</td>
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<td>T201108</td>
<td>F2-D2-HM-4</td>
<td>500-560,600-640</td>
<td>600-730</td>
<td>10.83/6.08</td>
<td>25/17</td>
<td>36-75</td>
<td>480-640/520-710</td>
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<td>14-26</td>
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<td>T201215</td>
<td>F2-S2-HMT-4</td>
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<td>460-550</td>
<td>10.88/6.54</td>
<td>22/26</td>
<td>43-80-99</td>
<td>440-640/530-700</td>
<td>18</td>
<td>17-24</td>
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<td>T201219</td>
<td>F2-S2-HM-4</td>
<td>480-560</td>
<td>450-550</td>
<td>10.52/5.8</td>
<td>35/37</td>
<td>36-66-112</td>
<td>480-557/540-690</td>
<td>25</td>
<td>17-24</td>
</tr>
</tbody>
</table>
Conclusion

- 3 concepts of PL SIR for TELIS have been proposed; 2 of them experimentally proven.
- SIR for TELIS has been developed, fabricated and preliminary tested.
- All main TELIS parameters are satisfied.
- A number of T2 chips with suitable parameters are selected for further RF measurements.
- Design and parameters of FFO and HM were optimized for TELIS.
- Possibility to operate a PL SIR remotely has been demonstrated.