SIS JUNCTION REACTANCE COMPLETE COMPENSATION

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Abstract

SIS junction geometrical capacitance together with out of phase current I_{kk} impedance component forms sufficient junction reactance $X_{SIS}=(\omega C+B_Q)^{-1}$. We suggested the way to resonate out both ωC and B_Q by using additional identical SIS junction connected to the first through a long line impedance invertor and RF+DC biased symmetrically to the first. Pumped IV curves without quantum reactance and frequency impedance patterns of the system were calculated. Calculations demonstrated the presence of high and even negative induced dynamic resistance regions at high order quasiparticle steps for the case of SIS junction reactance complete compensation. The suggested method may be used in SIS mixers and detectors for a better RF matching.

Introduction

One of the main problems in application of superconductor-insulator-superconductor (SIS) tunnel junctions in mm and sub mm mixers and detectors is the coupling of signal to the mixing element. Existence of considerable SIS junction susceptance which depends on geometric capacitance C_o and quantum susceptance B_Q which may be positive or negative and shunts the junction makes this problem not easy to solve [1,2].

It was found that for common SIS mixer operation Q-factor of SIS junction γ which is a product of frequency ω, junction capacitance C_o and normal resistance R_N : $\gamma=\omega R_N C_o$ must be 3-5 and it is necessary for good shunting of undesirable high frequency mixing components [3]. Therefore it means that the junction RF conductance G_Q is 1.5-2.5 times less than its susceptance. For short mm and sub mm wavelengths with increasing ω it is necessary to keep γ at optimal level and to reduce junction normal resistance R_N because for sandwich planar SIS junction topology the area of the junction are limited by the value 4-6 μm^2. This technological limitations are connected with the junction and its parameters reliability and reproducibility. Therefore SIS junction conductance G_Q increases and it aggravates the coupling problems. By now there were suggested three ways of solving this problem :

1. - to change the technology and to use edge junction topology, but this way has a few disadvantages - unique technology, low reliability of edge junctions with high R_N because of its sensitivity to electrical shocks [4] ;
2 - to use integrated inductive structures for resonating out junction susceptance [4,5,6];
3 - to use arrays of SIS junctions [7,8,9].

The real SIS mixers are tuned for lower conversion loss values only for the fixed bias voltage and LO power. It is very important for a proper SIS mixer operation to take into account the quantum susceptance B_Q. It should be very interesting and useful for the SIS mixer optimal operation to achieve compensation of the whole susceptance for arbitrary bias voltage V_o and LO power P_o. In the case of such complete compensation there is a possibility to find optimal SIS mixer operation conditions for bias voltage at the high order quasiparticle steps and therefore lower bias current I_o and hence less noise power. Calculations show that for high order steps bias SIS mixer operation and in the case of complete SIS junction susceptance compensation induced current steps with high and even negative resistance appear and it is possible to realize the conversion with amplification.

SIS junction performance under microwave radiation in the case of complete SIS junction susceptance compensation

Practical SIS mixers and detectors are tuned only for concrete values of frequency, LO power and dc bias. In this case it is possible to achieve conversion with amplification if the sum susceptance of system SIS junction-embedding network equals zero. Changes of bias voltage V_o or LO power lead to changes of the junction quantum conductance G_Q and quantum susceptance B_Q and thus SIS mixer or detector detunes. That is the reason why the SIS mixer at high order steps dc bias ($V_o=V_g-(n+1/2)hf/e$, $n\geq 1$, e - electron charge, h - Plank constant, V_g - gap voltage) has poor coupling to input signal. Calculations and experimental results of this case see in ref.[2].

If we suppose that it was achieved complete SIS junction susceptance compensation (CSC) for arbitrary bias and LO power then the SIS junction IV curve with LO power irradiation changes dramatically. Fig.1 shows the calculated IV curves and normalized amplitude of RF voltage $\alpha=eV_{RF}/hf$ versus bias voltage for different LO power levels and for different LO source resistance R_S (a,b,c). In calculations we used typical IV curve (lower curve in Fig.1). The most important difference of CSC in comparison with the common operation of SIS junction is the presence of induced high and even negative differential resistance at the second and third quasiparticle steps.

Therefore in the case of CSC high order quasiparticle steps biased SIS junction may be used for mixing with increased quantum resistance $R_Q=(0.3-0.5)R_j$, here $R_j=(15-30)R_o$ leakage resistance. Additional advantage of high order steps bias operation mode is the decreasing of bias current I_o and reducing of shot noise $I_n^2=2eI_o\Delta f$, here Δf is IF bandwidth.

Complete SIS junction susceptance compensation realization

The most important feature of SIS junction susceptance is its dependence on bias voltage and LO power. Therefore it is impossible to realize CSC by using of permanent inductive components to resonate out susceptance. It is necessary to use flexible compensation following the susceptance changes. To solve this problem we propose to use additional SIS junction which is identical to the first one, biased and pumped symmetrically. If we connect the first SIS

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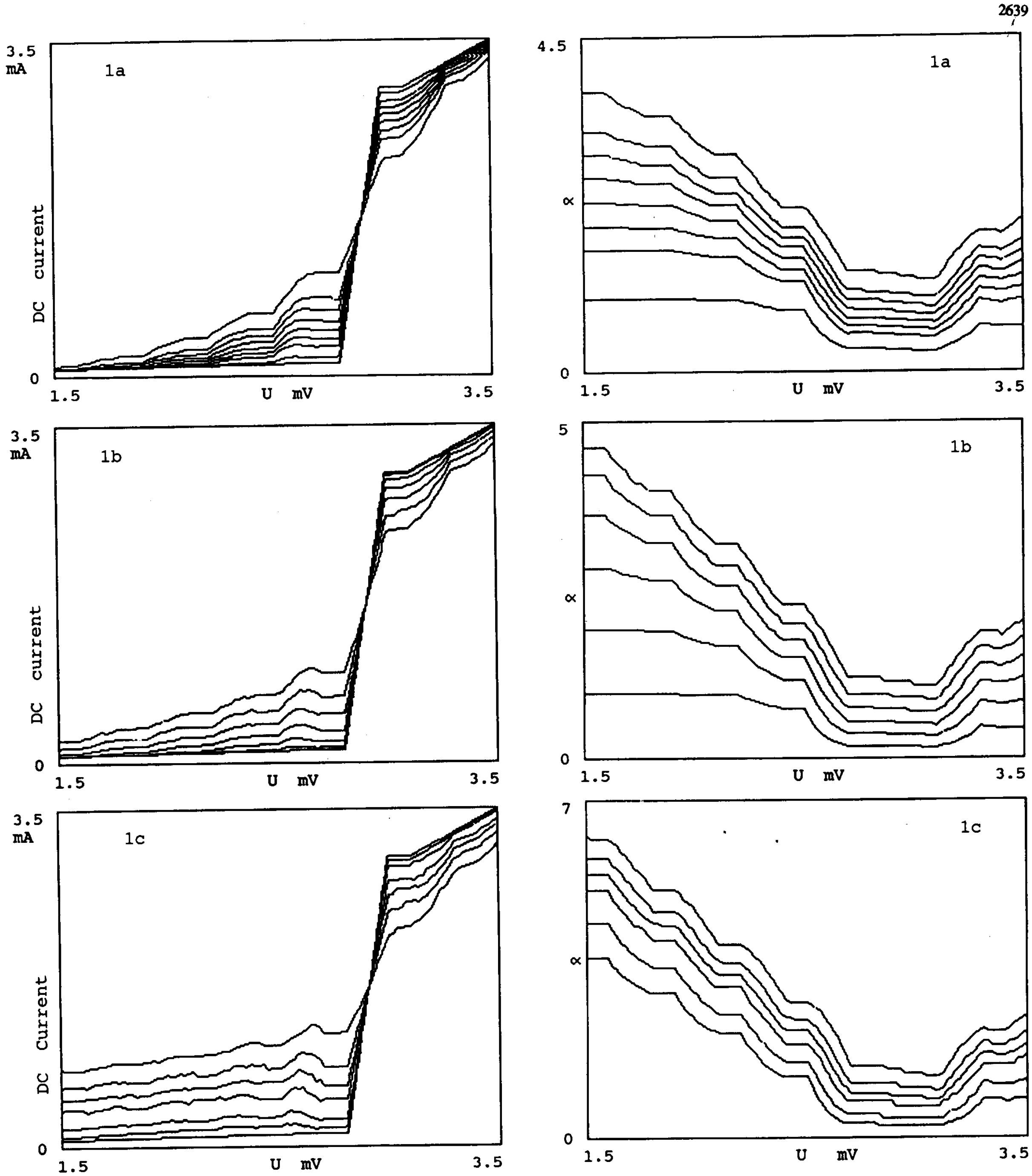

Fig.1. Calculated IV curves and normalized RF amplitude across the junction versus bias voltage for different LO power levels and different LO source output resistances R_s

a. $R_s/R_N=0.5$

b. $R_s/R_N=1$

c. $R_s/R_N=5$

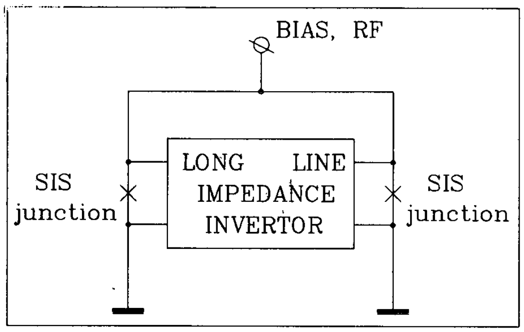

Fig.2. SIS junction bias and LO power circuits and long line impedance invertor connections for complete susceptance compensation.

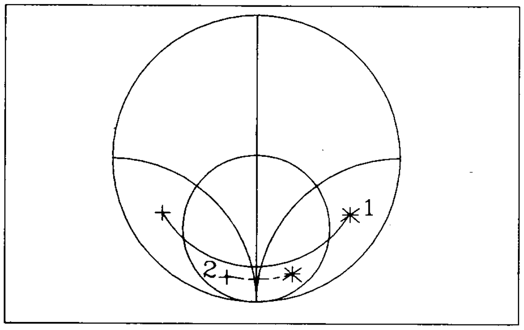

Fig.3. Smith's chart impedance invertor illustration. The star on the chart is the SIS junction admittance. The cross is the output admittance after invertor. Curves 1,2 show different long line impedances $R_{01}<R_{02}$

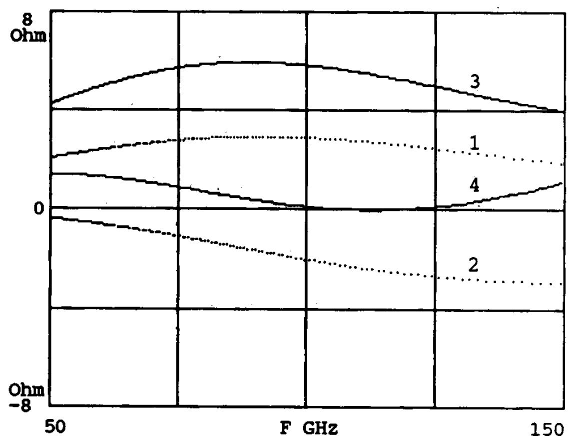

Fig.4. Calculated SIS junction direct detector input impedance as a function of frequency f. Curves 1,2 present real and imaginary parts of single SIS junction input impedance, curves 3,4 - real and imaginary parts of the same two SIS junctions RF series connected by impedance invertor (twins compensation).

junction to the secondary via long line with proper length l, then at some frequency ω this long line will be impedance invertor and we shall have pure real impedance at the end of the line. Fig.2 presents illustration of junctions connections, bias and pump circuits. It should be noted that because of junctions full identity bias and pumping circuits may be of parallel or series types for better matching.

Fig.3 shows Smith's chart and illustrates flexible compensation. The star on the diagram corresponds to SIS junction admittance and the cross is the final output admittance at the end of long line impedance invertor. The arc situated between the star and the cross corresponds to the electrical length of impedance invertor. Long line impedance R_1 defines the frequency band of the system. With R_1 increase geometric sizes decrease (the dashed line on Smith chart Fig.3).

Calculated real and imaginary parts of SIS direct detector input impedance for a single SIS junction (1,2) and the same two junctions RF series connected via microstrip impedance transformer (3,4) are shown in Fig.4. Calculations were made for 3-port SIS junction operation mode because very wide frequency band of such twin compensation in real devices would be reduced by waveguide or embedding circuit and higher harmonics may be ignored.

The self compensated distributed SIS junctions array based on set of such pairs of SIS junctions connected via impedance invertor should be compatible for short mm and sub mm wavelengths mixers.

The experimental verification of complete SIS junction susceptance compensation would be the observation of high or negative induced steps resistance at high order steps under microwave irradiation. IV curves of series SIS arrays with parallel bias [10] demonstrate such anomalous behavior. Analysis of the array topology shows that for some frequencies it may be viewed as shown in Fig.2. More information about array topology and experimental studies of mixers see in this book [11].

Conclusion

We suggested a new method of complete SIS junction reactance compensation when both the junction capacitance and quantum reactance are resonated out by means of connecting additional SIS junction via long line impedance invertor. In this case it is possible to improve SIS mixer performance by achieving mixing with amplification at higher order steps bias. In mm and sub mm mixers it is possible to use such method for design the self compensated distributed SIS junctions arrays.

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